UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :None Installed
UMA:UMA platform installed
OPS:Optimus
HR:Huron River
CRV:Chief River

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A3	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 1 of 103	

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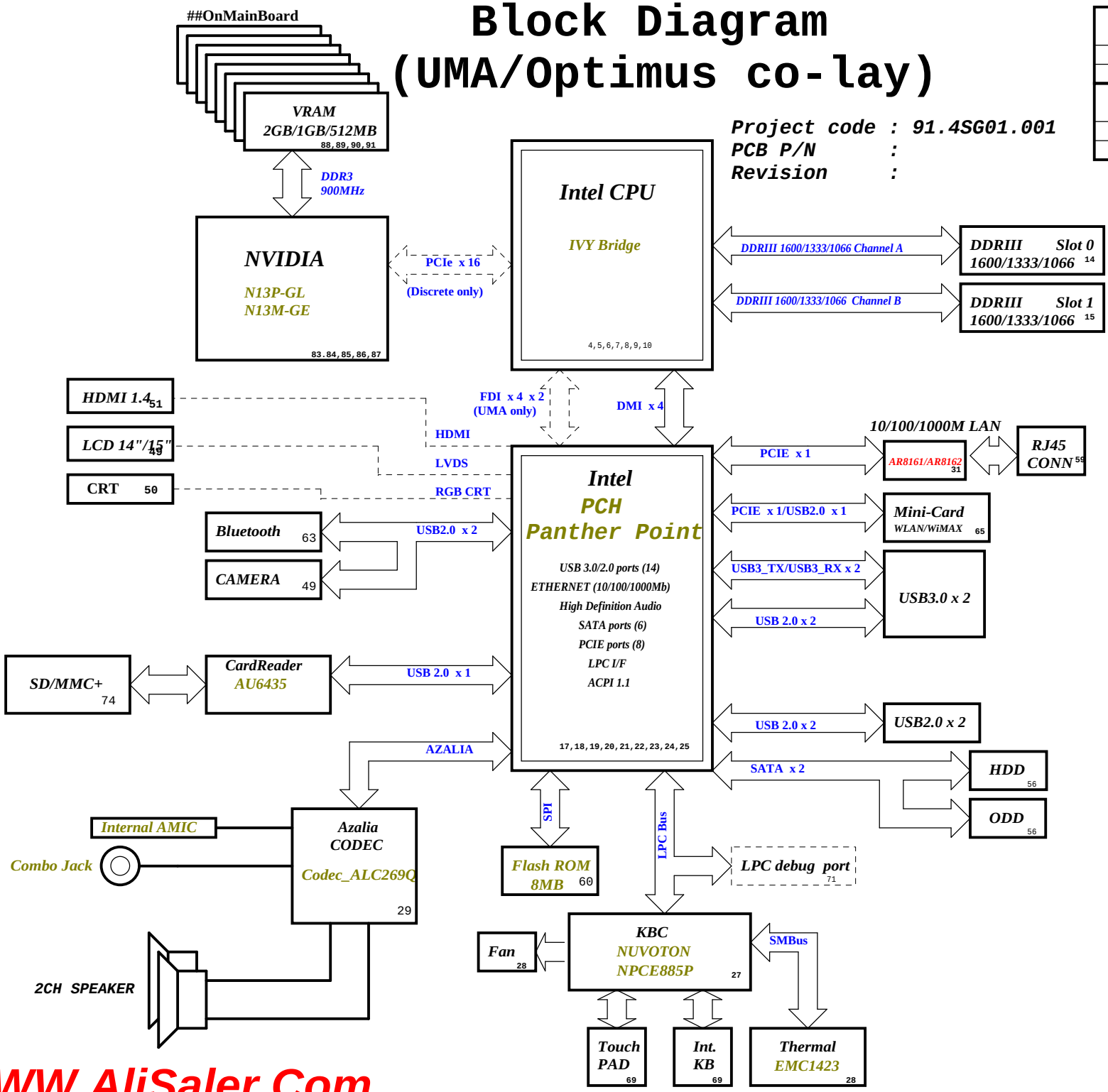
Block Diagram (UMA/Optimus co-lay)

##OnMainBoard

Project code : 91.4SG01.001
PCB P/N :
Revision :



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
DCBATOUT	VCCSA

SYSTEM DC/DC TPS51211 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

CPU DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC G977F 45	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S0

SYSTEM DC/DC TPS51123 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC TPS51640RSLR 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA ISL62882C 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24745 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

VGA switchs 93	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D05V_VTT	1D05V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

JV10-CS

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Title: Block Diagram

Size	Document Number	Rev
A3	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 2 of 103

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

All Not update

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	N/A
1	HDD1
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	X
1	USB3.0 ext port 1
2	USB2.0 ext port 4
3	USB3.0 ext port 2
4	BLUETOOTH
5	CARD READER
6	X
7	X
8	X
9	USB2.0 ext port 3
10	X
11	WLAN(Bluetooth)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

JV10-CS

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Title: mTable of Content

Size: A3 | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 3 of 103

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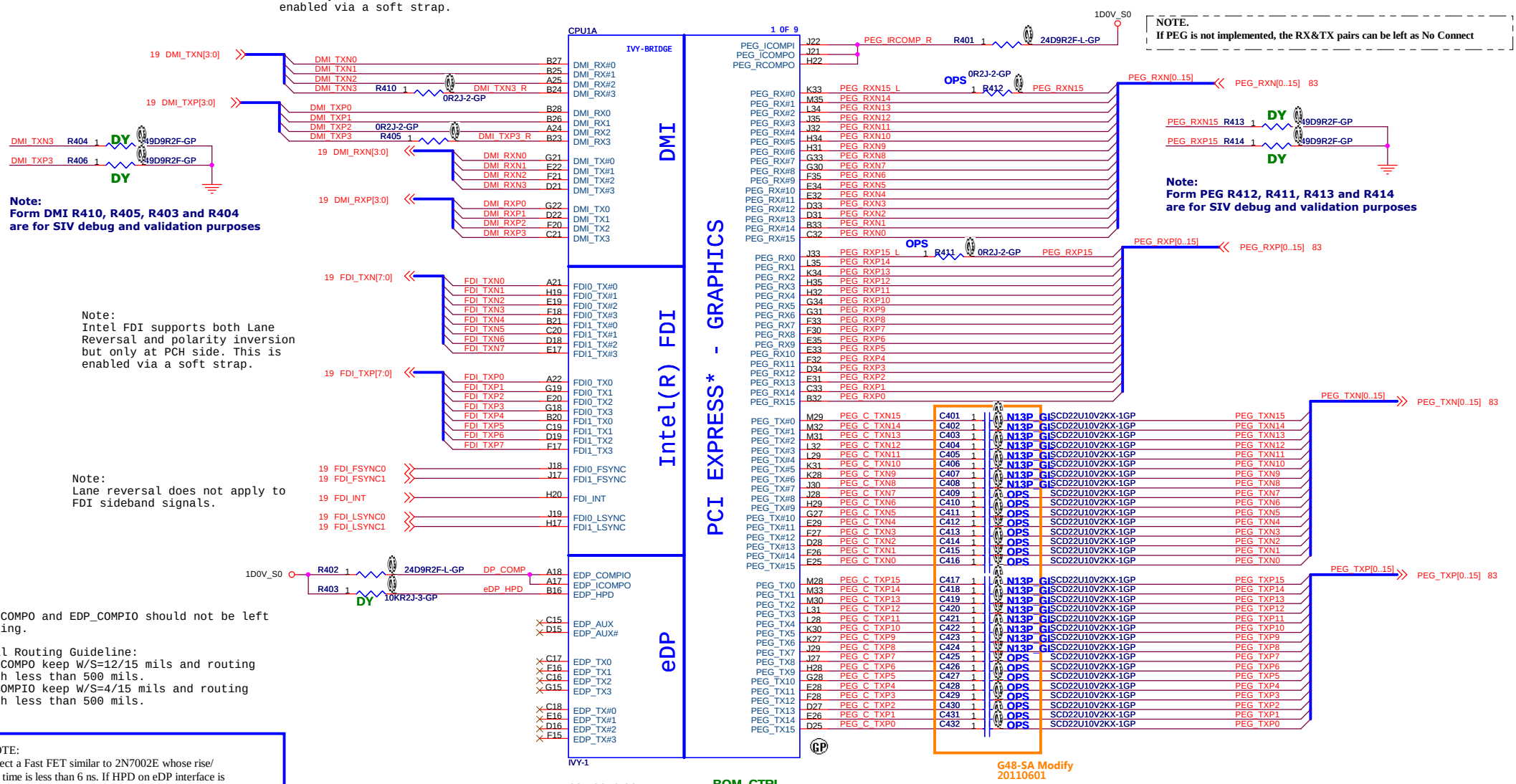
SSID = CPU

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Form DMI R410, R405, R403 and R404 are for SIV debug and validation purposes

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Note:
EDP_ICOMPO and EDP_COMPIO should not be left floating.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Note:
Form PEG R412, R411, R413 and R414 are for SIV debug and validation purposes

G48-SA Modify
20110601

62.10040.821

1st = 22.10252.171

2nd = 62.10040.821

3rd = 62.10055.551

BOM_CTRL

JV10-CS

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Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 4 of 103	

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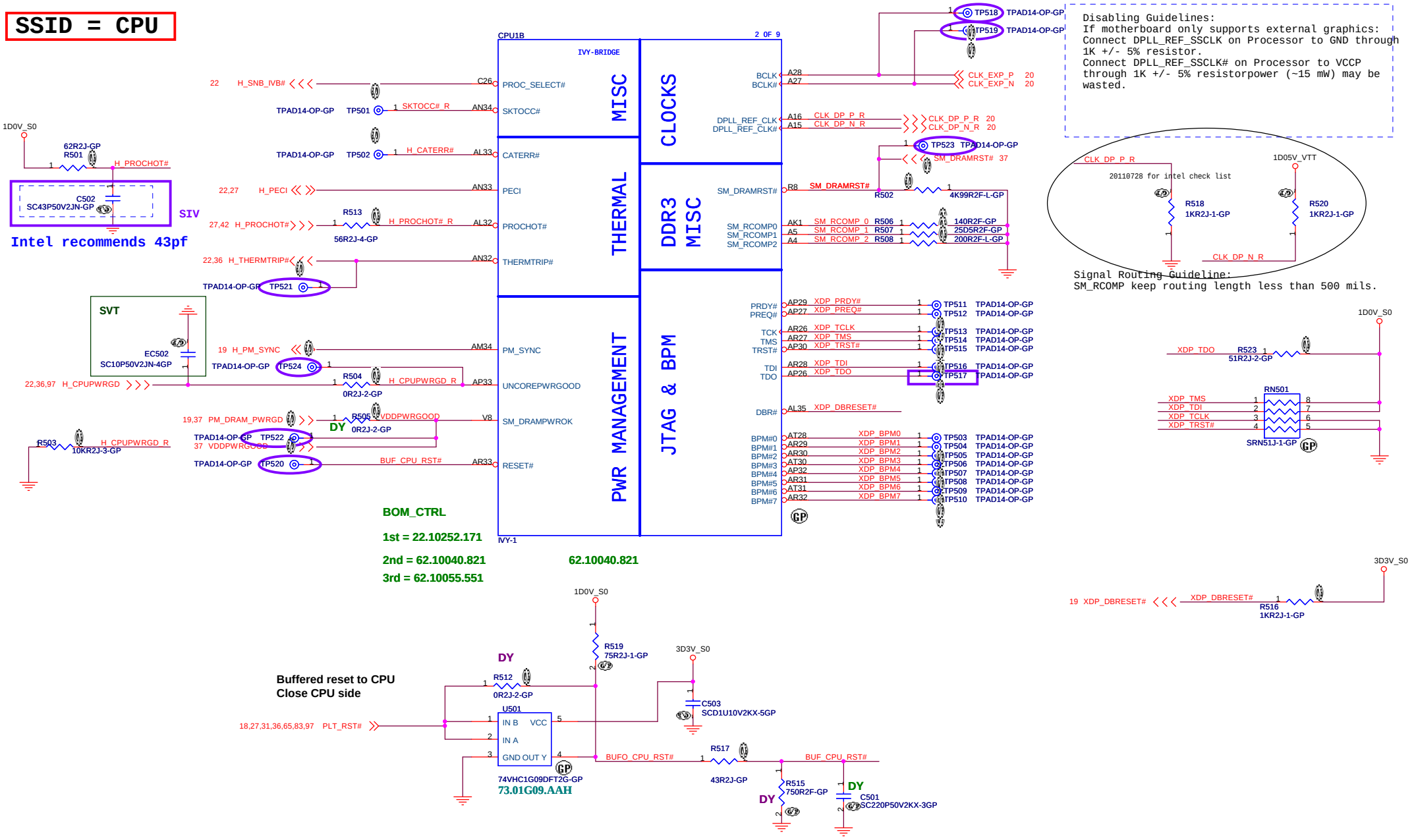
SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Buffered reset to CPU
Close CPU side

NOTE

	U501	R512	R519	R517	R515	C503	C501
HR	DY	0 ohm 63.R0034.1DL	DY	1.5K ohm 64.15015.6DL	750 ohm 64.75005.6DL	DY	DY
CRV	73.01G09.AAH	DY	75 ohm 63.75034.1DL	43 ohm 63.43034.1DL	DY	0.1uF 78.10423.2FL	DY

Default CRV

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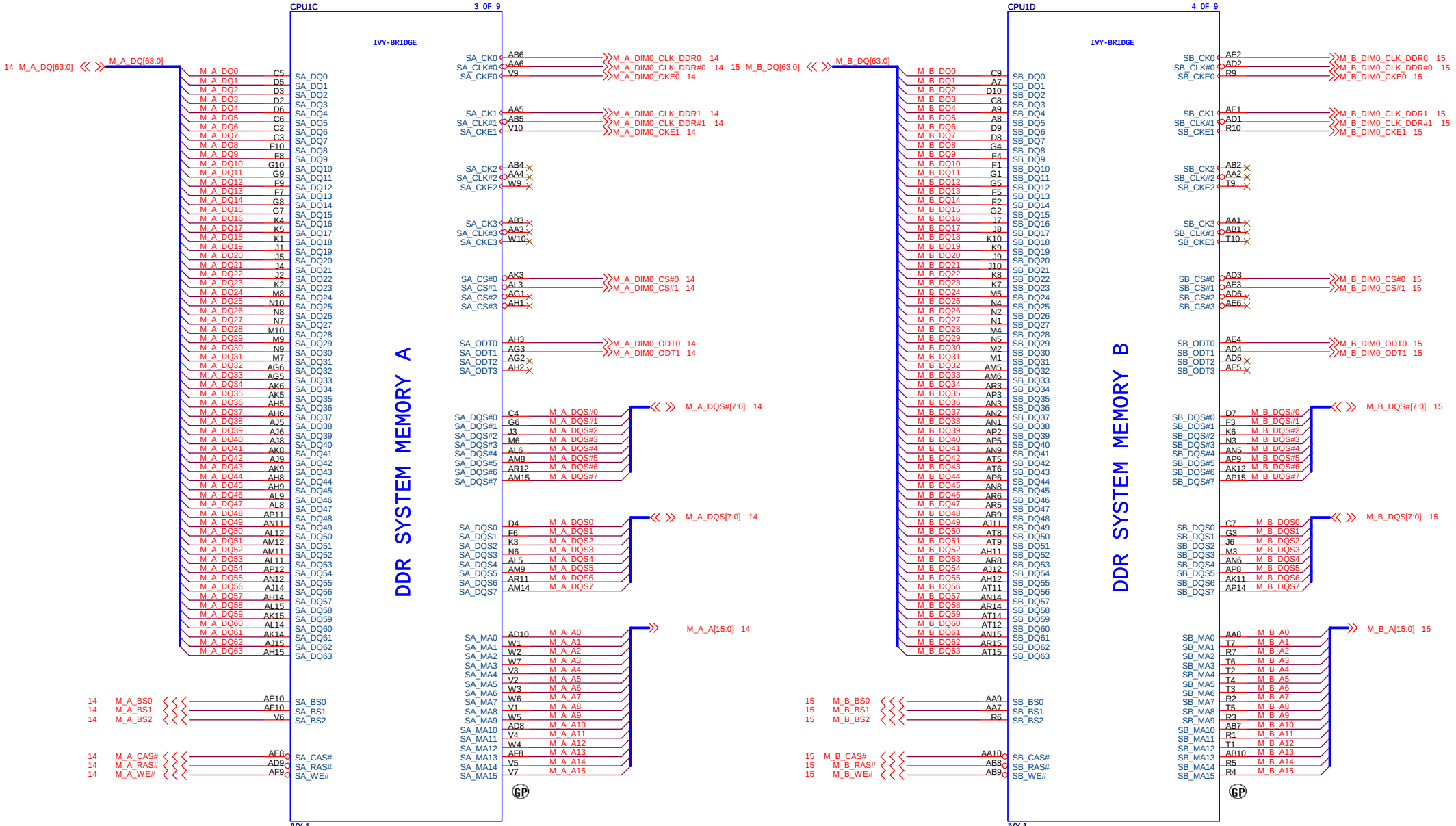
Title: THERMAL/CLOCK/PM

Size: A3 | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 5 of 103

SSID = CPU



62.10040.821

BOM_CTRL

1st = 22.10252.171
2nd = 62.10040.821
3rd = 62.10055.551

62.10040.821

BOM_CTRL

1st = 22.10252.171
2nd = 62.10040.821
3rd = 62.10055.551

緯創資通 **Wistron Corporation**
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Title			
CPU (DDR)			
Size A3	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 6 of 103		

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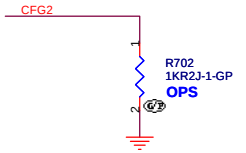
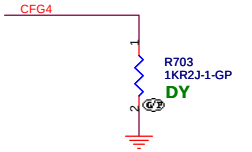
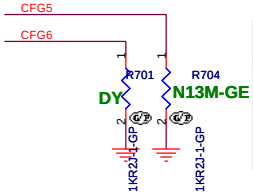
SSID = CPU



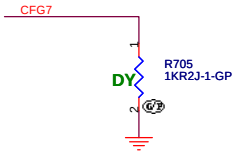
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



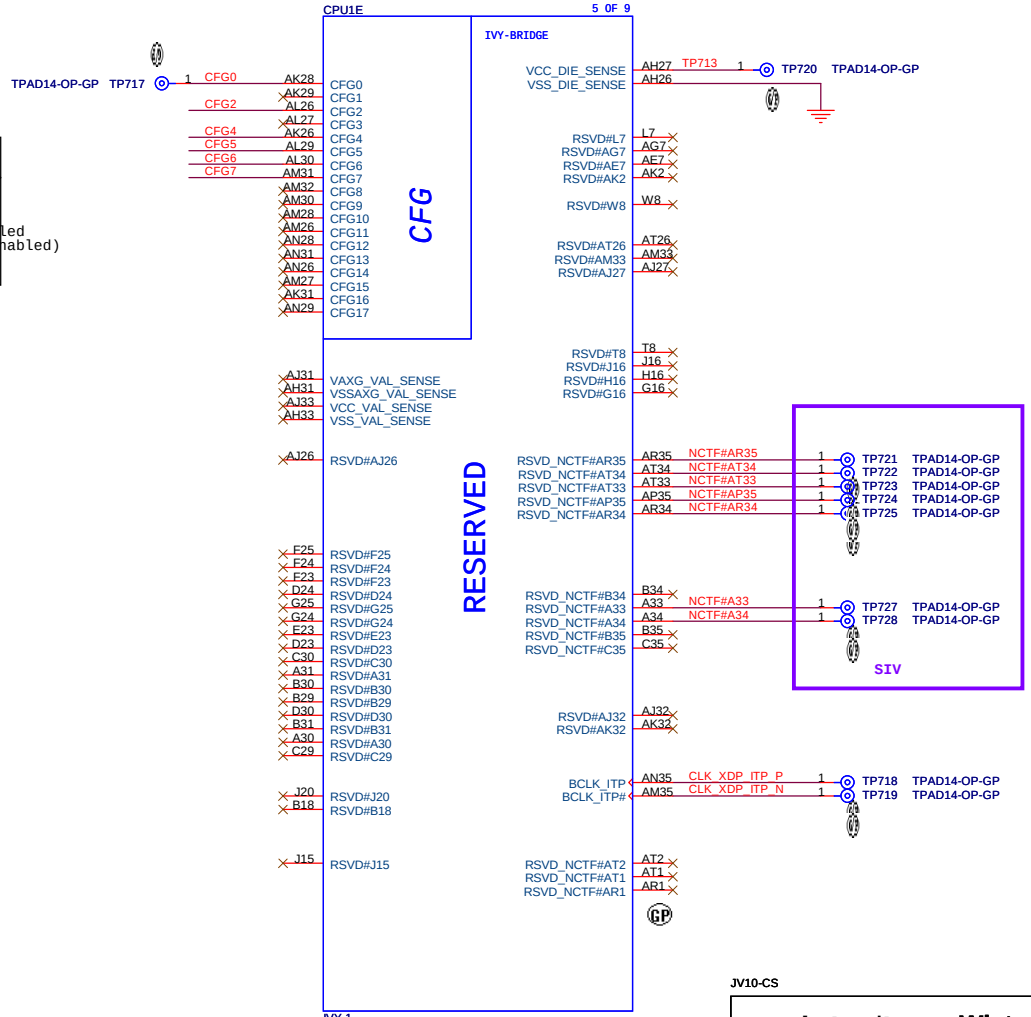
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



IVY-1

62.10040.821

BOM_CTRL

JV10-CS

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Title: CPU (RESERVED)		
Size: A3	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 7 of 103	

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SSID = CPU

POWER

CPU1F

6 OF 9

IVY-BRIDGE

VCC_CORE

VCC CORE:53A

SC10U6D3V5KX-1GP

DY

VCCIO:8.5A

1D0V_S0

-to 17pcs

TC8xx

470uF x2

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

R807 need to close to CPU

R807 75R2F-2-GP

110722 Ge

R808 10R2F-L-GP

R809 10R2F-L-GP

VCCIO_SENSE

VSSIO_SENSE

VIDALERT# H_CPU_SVIDALRT# R803 43R2J-GP VR_SVID_ALERT# 42

VIDSCLK H_CPU_SVIDCLK_R R805 0R2J-2-GP H_CPU_SVIDCLK 42

VIDSOUT H_CPU_SVIDDAT_R R806 0R2J-2-GP H_CPU_SVIDDAT 42

R804 130R2F-1-GP

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7

For CRB VIDALERT# need to pull high 75 ohm close to CPU

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

VCC_SENSE AJ35

VSS_SENSE AJ34

VCCSENSE 42

VSSSENSE 42

VCCIO_SENSE B10 VCCIO_SENSE TP802 TPAD14-OP-GP

VSS_SENSE_VCCIO A10 VSSIO_SENSE TP803 TPAD14-OP-GP

BOM_CTRL

IVY-1

62.10040.821

JV10-CS

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Title: mCPU (VCC_CORE)

Size: Custom | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 8 of 103

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SSID = CPU

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

POWER

M3 - Processor Generated SO-DIMM VREF_DQ

M_VREF_DQ_DIMM0 — R915 1 — DY — 0R2J-2-GP
M_VREF_CA_DIMM0 — R916 1 — DY — 0R2J-2-GP
RN903 SRN1KJ-7-GP DY
12 DDR_WR_VREF01
12 DDR_WR_VREF02

VCC_GFXCORE

CPU1G 7 OF 9 IVY-BRIDGE

GRAPHICS: AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17
VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

C901 C902 C903 C904 C905 C906 — SC10U6D3V5KX-1GP — RC901 SC33P50V2JN-3GP DY
C907 C908 C918 C919 C920 C921 — SC10U6D3V5KX-1GP — RC902 SC33P50V2JN-3GP DY

SENSE LINES
VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF
SM_VREF AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37
SA_DIMM_VREFDQ B4
SB_DIMM_VREFDQ D1

DDR3 -1.5V RAILS
VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AE1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

PROCESSOR VDDQ: 12A
C909 C910 C911 C912 C913 C914 — SC10U6D3V5KX-1GP
SIV — 1D5V_S0 — TC902 ST330U2D5VDM-17GP — DY
TC9xx 330uF

SA RAIL
VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

PROCESSOR VCCSA: 6A
VCCSA
C916 C915 C917 — SC10U6D3V5KX-1GP
TC9xx 330uF

R902 need be close to pin H23.

MISC
VCCSA_SENSE H23 — VCCSA_SENSE — VCCSA_SENSE 48
VCCSA_VID0 C22 — VCCSA_SELECT0 48
VCCSA_VID1 C24 — VCCSA_SELECT1 48
VCC_IO_SEL A19 — GP

1.8V RAIL
VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

1D8V_S0
VCCPLL:1.5A
C925 C923 — SC10U6D3V5KX-1GP
C922 C924 — SC1U10V2KX-1GP
TC9xx 330uF

IVY-1

62.10040.821

BOM_CTRL
SIV
3D3V_S5 — R913 10KR2F-2-GP — DY
ES2 dummy R913
H_VCCIO_SEL

1D0V_S0
R917 10KR2J-3-GP DY — VCCSA_SELECT0
R920 10KR2J-3-GP DY — VCCSA_SELECT1
R918 1KR2J-1-GP
R919 1KR2J-1-GP
SIT

Close to CPU
VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U
SIV for intel recommend

NOTE

	R906/R907
HR	100 ohm 64.10005.6DL
CRV	10 ohm 64.10R05.6DL

Default CRV

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Title	mCPU (VCC_GFXCORE)	
Size A3	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 9 of 103	

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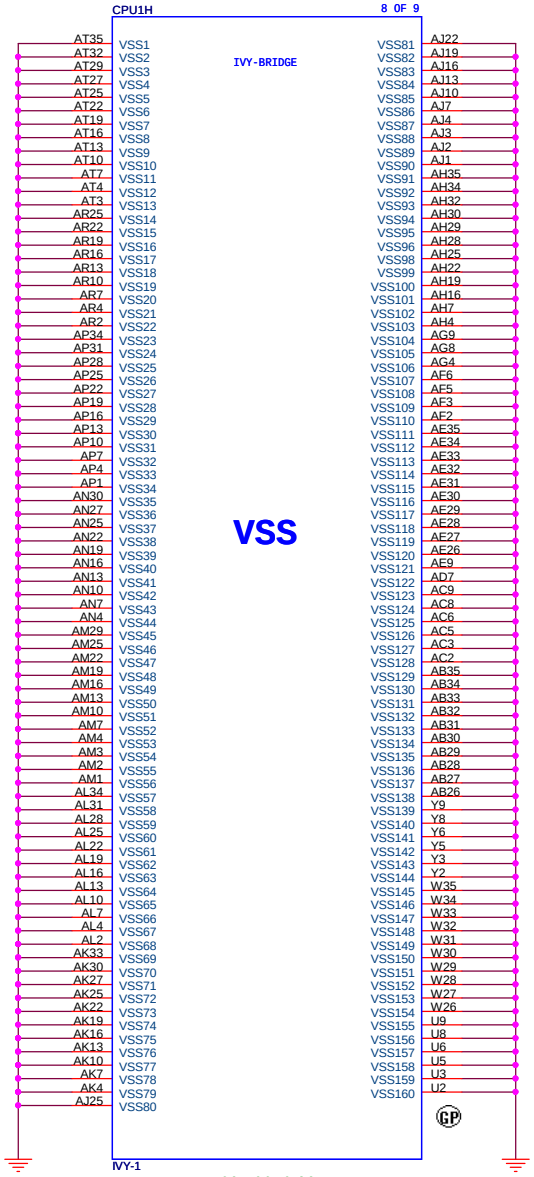
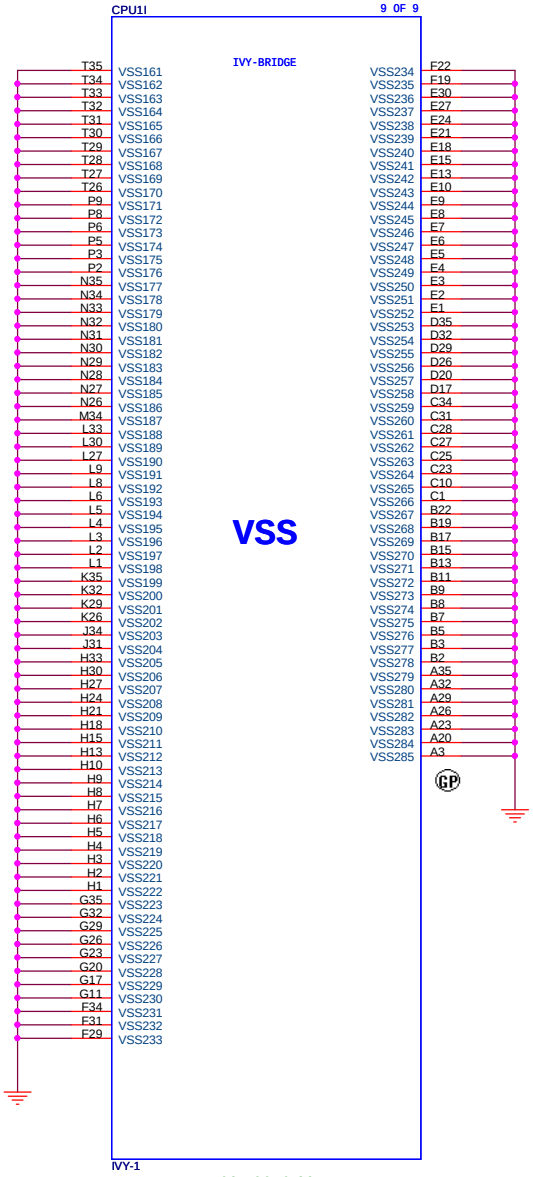
SSID = CPU



62.10040.821

BOM_CTRL



62.10040.821

BOM_CTRL

JV10-CS

緯創資通 Wistron Corporation
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Title	CPU(VSS)	
Size A3	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 10 of 103	

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JV10-CS

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Title	***XDP***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 11 of 103	

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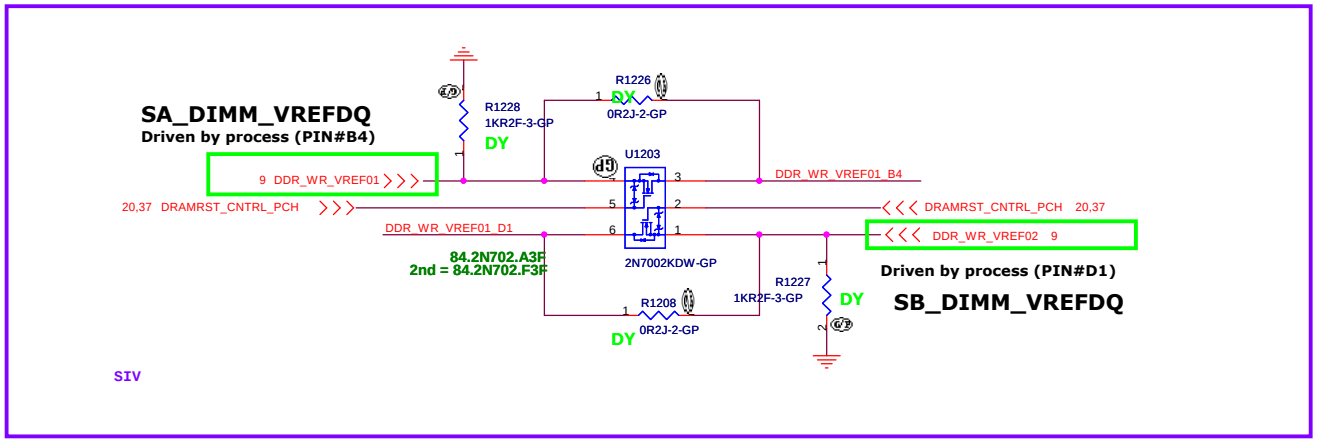
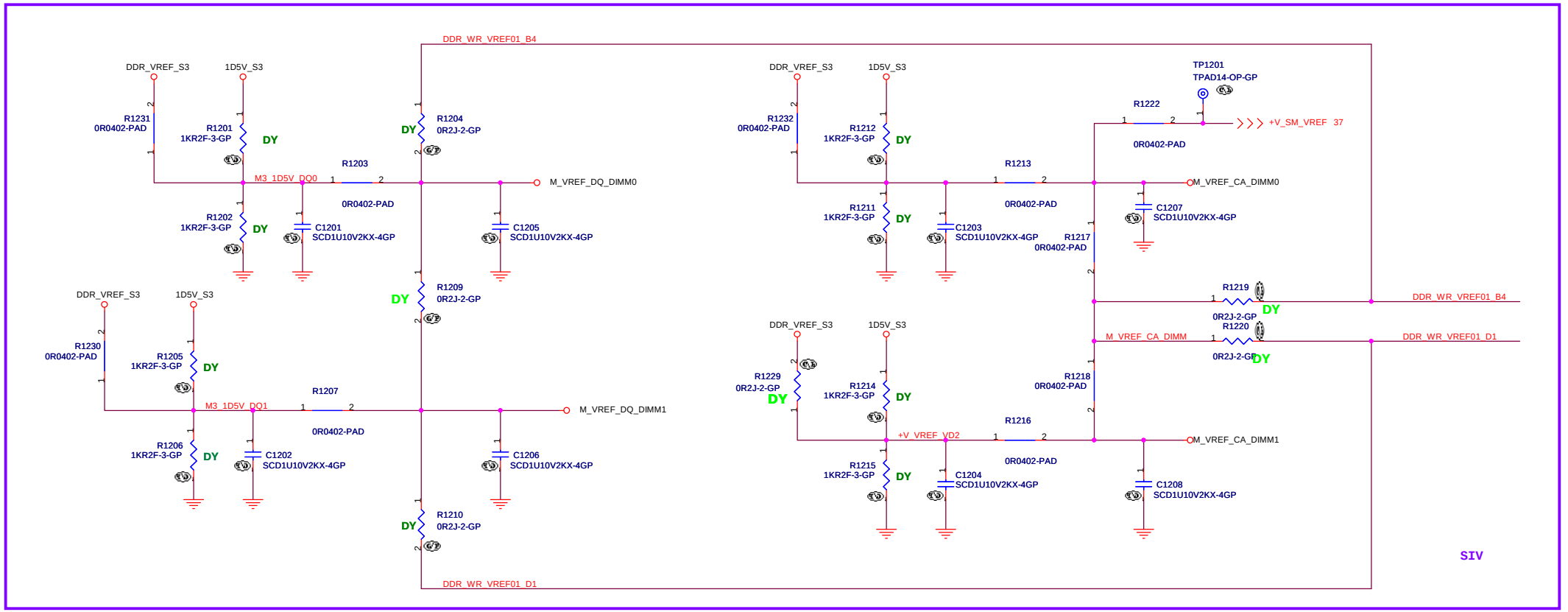
VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

For CRV:





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Title: *M1 & M3 Implementation*		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 12 of 103	

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Title	***Reserved***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 13 of 103	

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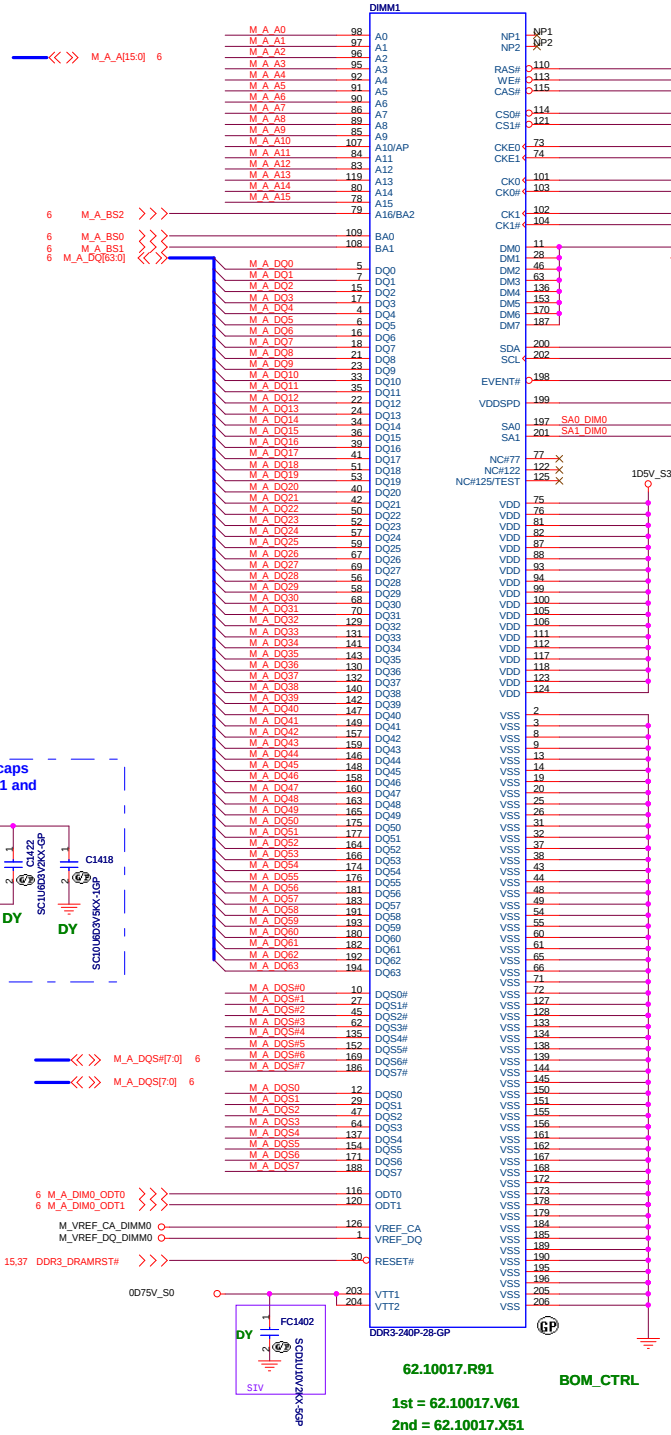
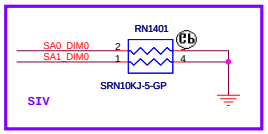
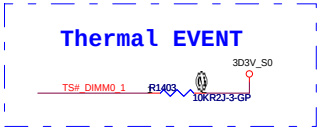
SSID = MEMORY

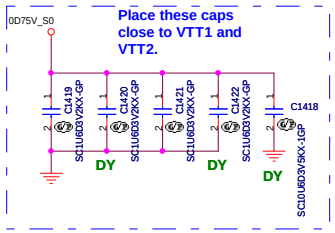




Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32





62.10017.R91

1st = 62.10017.V61
2nd = 62.10017.X51
3rd = 62.10017.R91

BOM_CTRL

After layout, BOM change P/N

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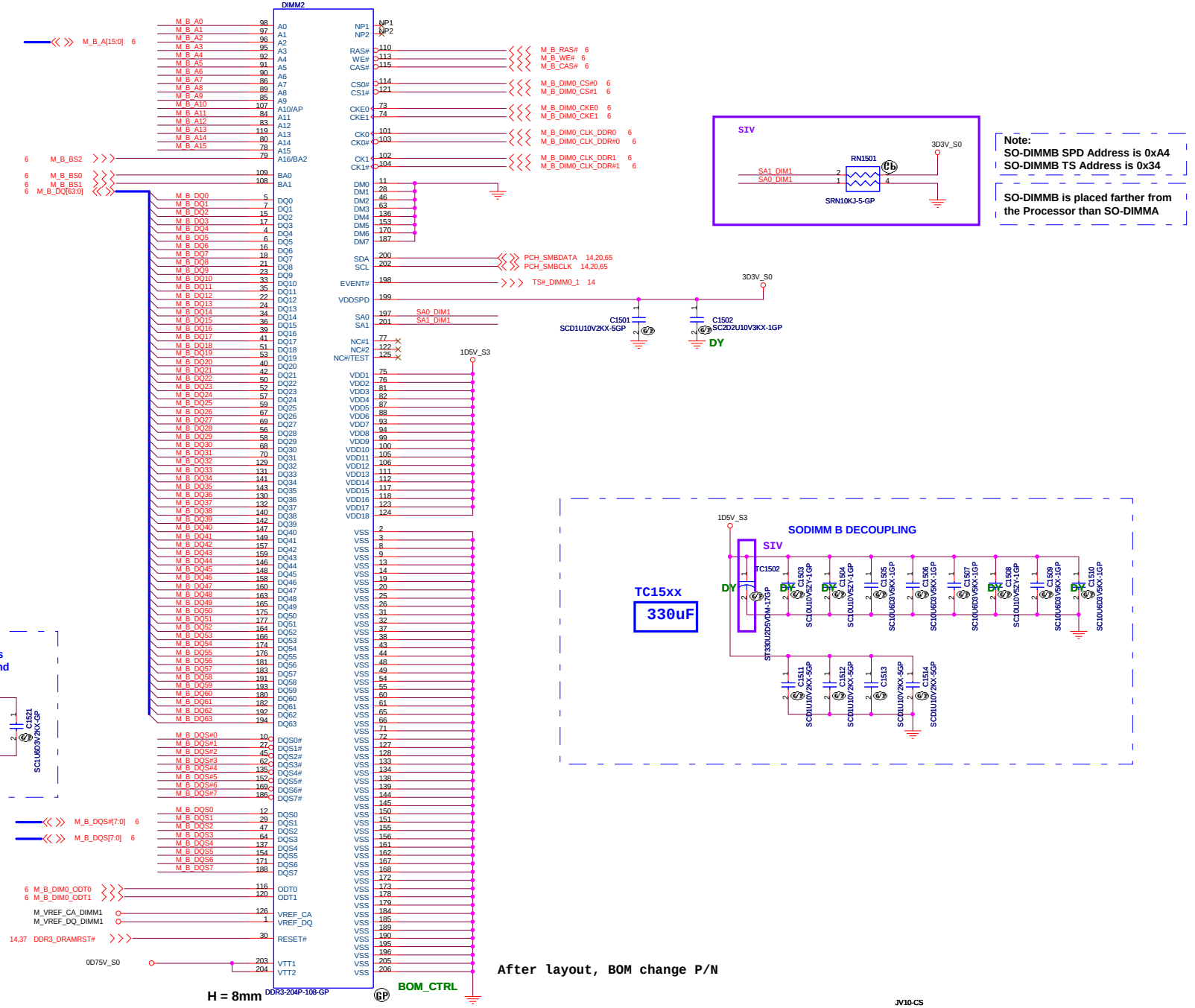
Title: **DDR3-SODIMM1**

Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 14 of 103

SSID = MEMORY



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Title: DDR3-SODIMM2

Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 15 of 103

(Blanking)

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Title	DDR3-SODIMM3	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 16 of 103	

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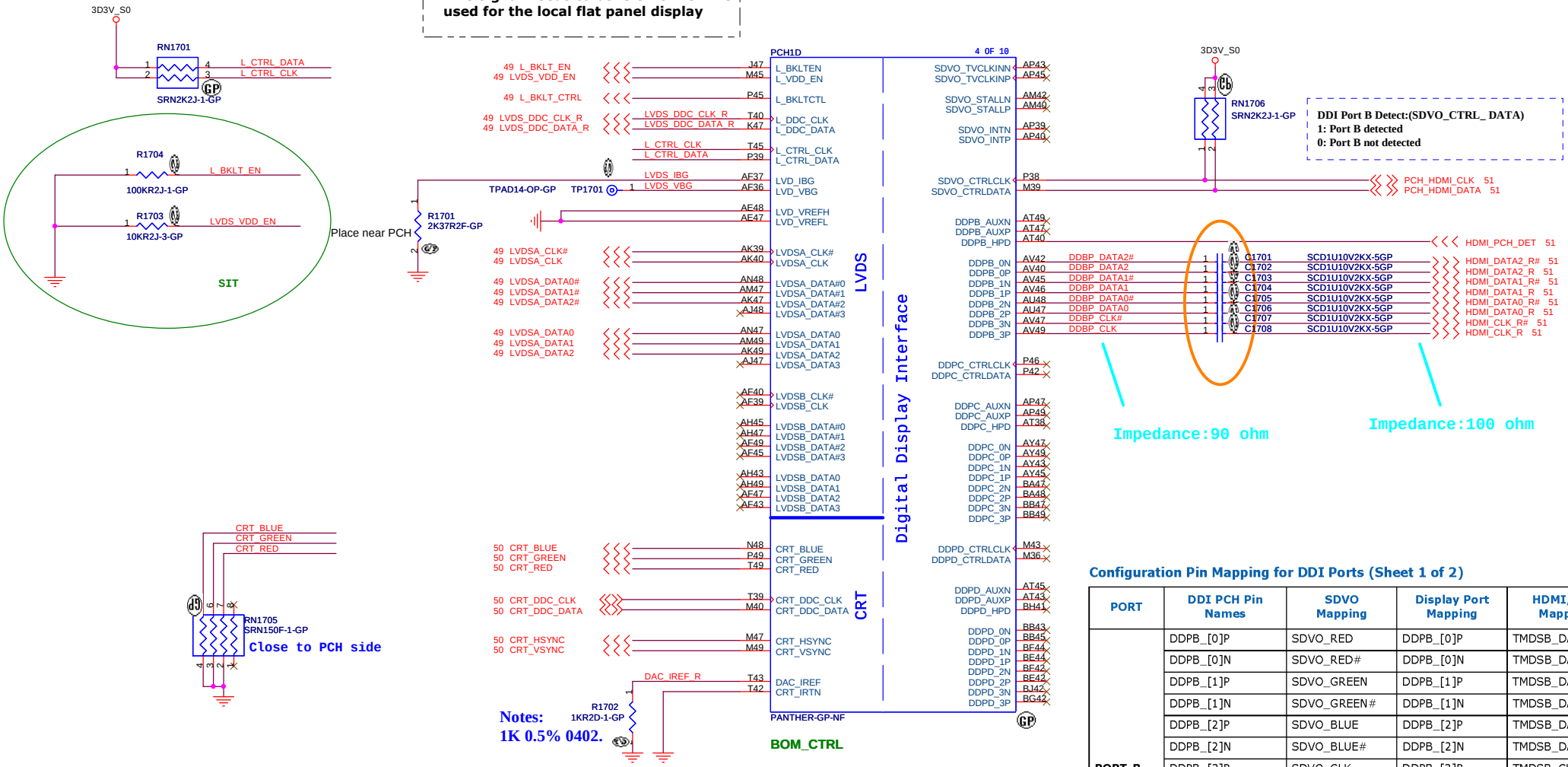
L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is used for the local flat panel display



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

Digital Display Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
LVDS	L_DDC_DATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

NOTE: LVDS and eDP on processor can not be enabled at the same time.

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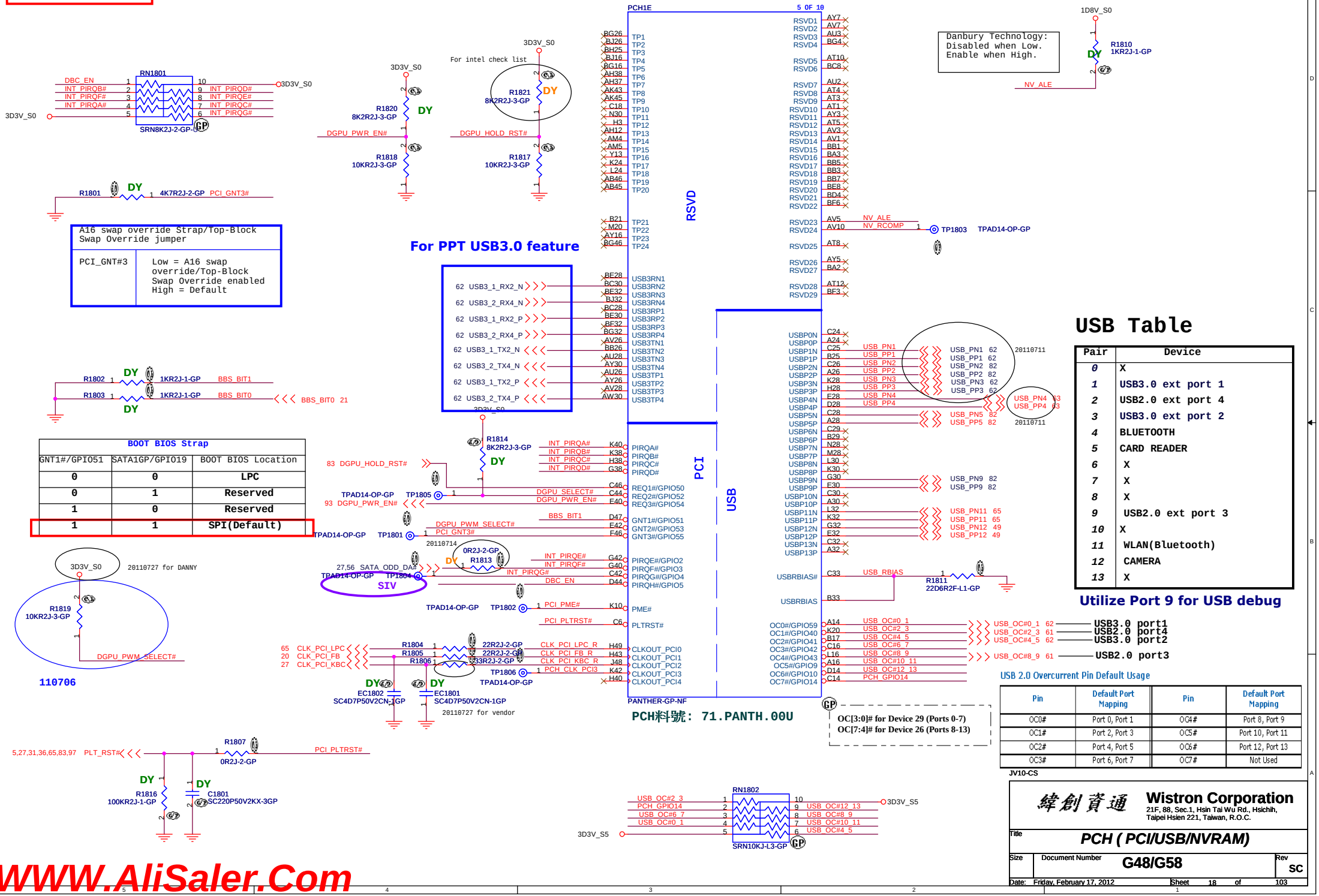
Title: **PCH (LVDS/CRT/HDMI)**

Size | Document Number: **G48/G58** | Rev: **SC**

Date: Friday, February 17, 2012 | Sheet 17 of 103

SSID = PCH



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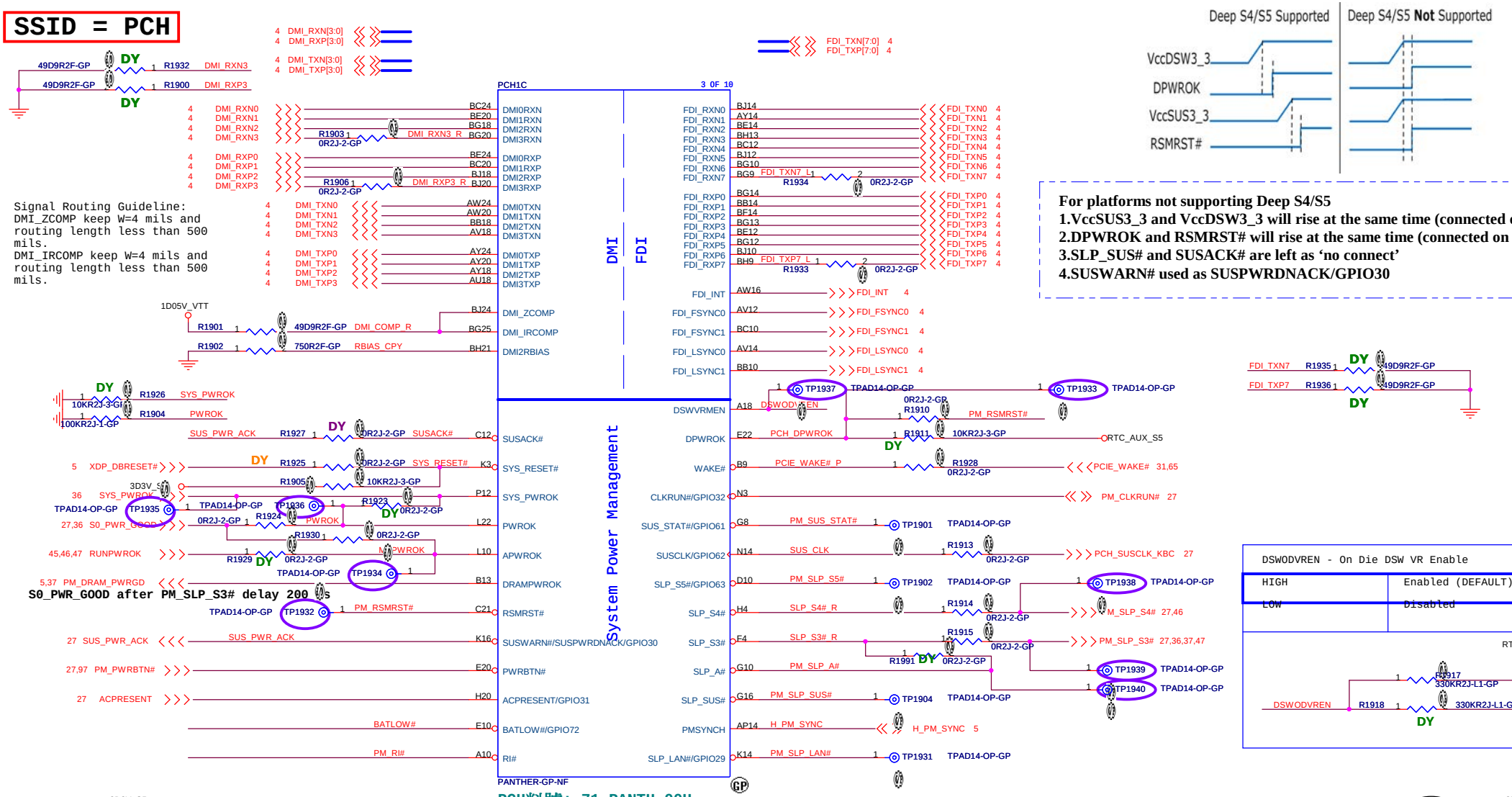
SSID = PCH



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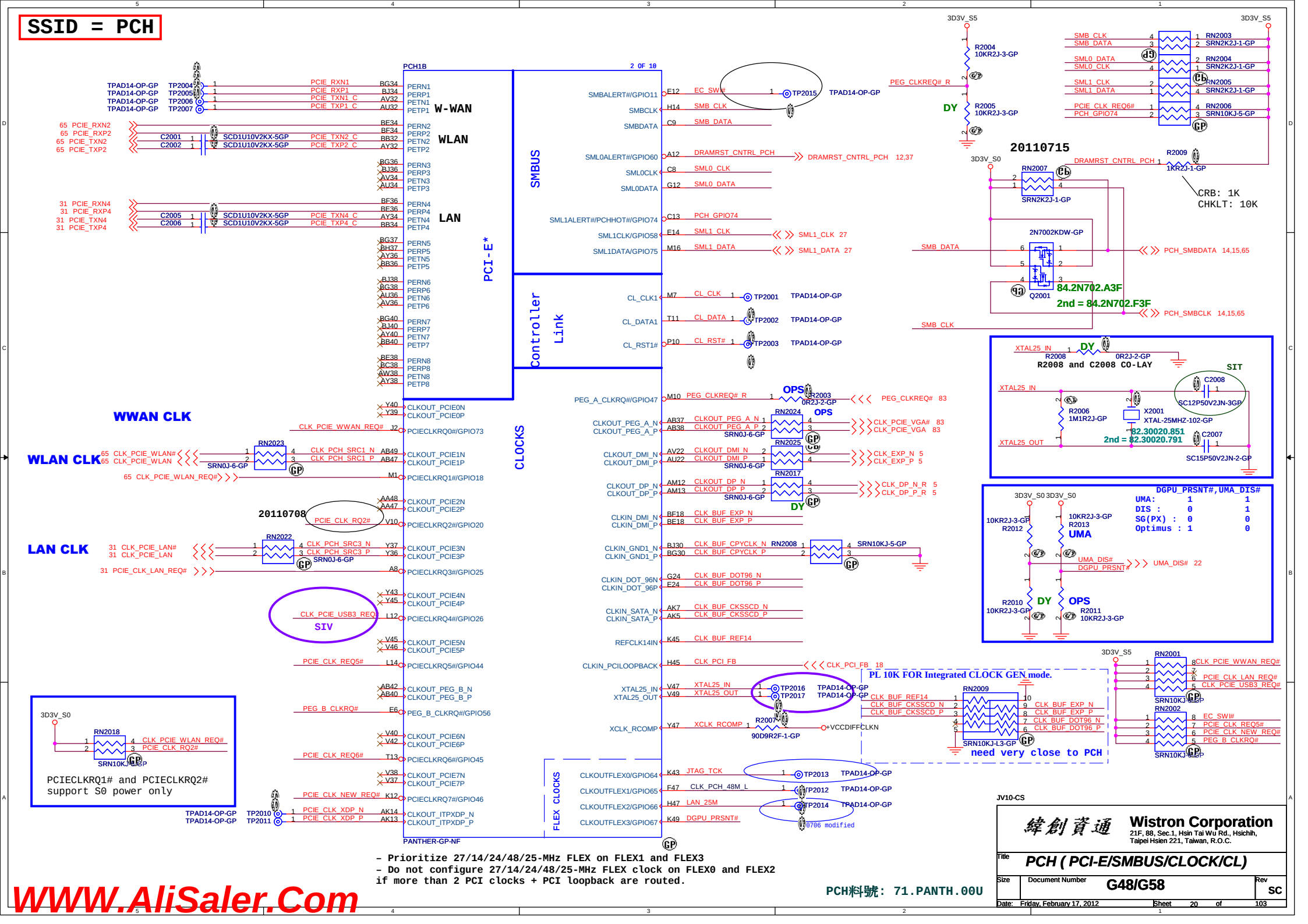
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DMI/FDI/PM)

Size: | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 19 of 103

SSID = PCH



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SSID = PCH

NOTE

	R2111,R2118~R2120,R2125
HR	0 ohm 63.R0034.1DL
CRV	22 ohm 64.22R05.6DL

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide

HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V (Default) High = 1.5V

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

Move Cap close to Device or Connector.

LA37/LA57/CRV-Std:750ohm
LA47: 806 ohm

PCH料號: 71.PANTH.00U

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JV10-CS

110706 modified

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (SPI/RTC/LPC/SATA/IHDA)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 21 of 103	

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

Note

	R2202	----
HR	200K ohm 64.20035.6DL	
CRB	10K ohm 63.10334.1DL	

PCH_GPIO15 pull high => HM76
PCH_GPIO15 pull Low => HM70

LOW: ODD exist
HIGH: ODD non-exist

PCH料號: 71.PANTH.00U

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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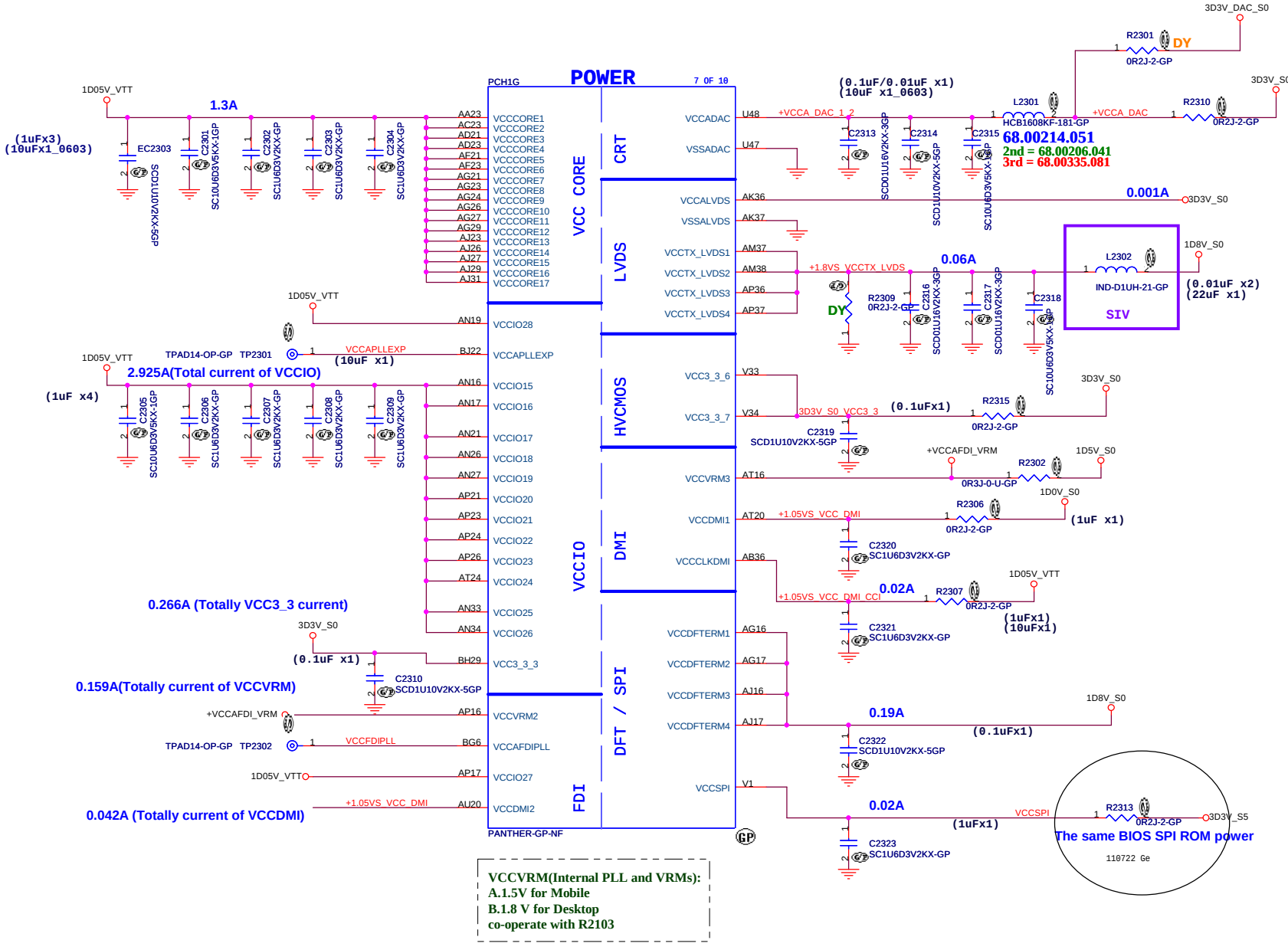
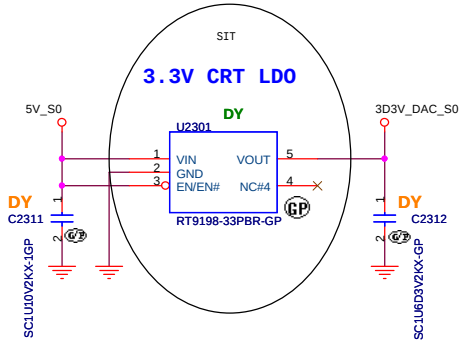
Title: PCH (GPIO/CPU)
Size: | Document Number: G48/G58 | Rev: SC
Date: Friday, February 17, 2012 | Sheet 22 of 103

SSID = PCH 6A





Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture

VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with R2103

JV10-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 23 of 103

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SSID = PCH

POWER

PCH1J — 10 OF 10

after layout, place 4.7uF *3

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM)

0.097A (Totally current of VCCSUS3_3)

0.001A

0.002A

0.08A

0.055A

0.095A

0.01A

6uA

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

PANTHER-GP-NF

JV10-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 24 of 103

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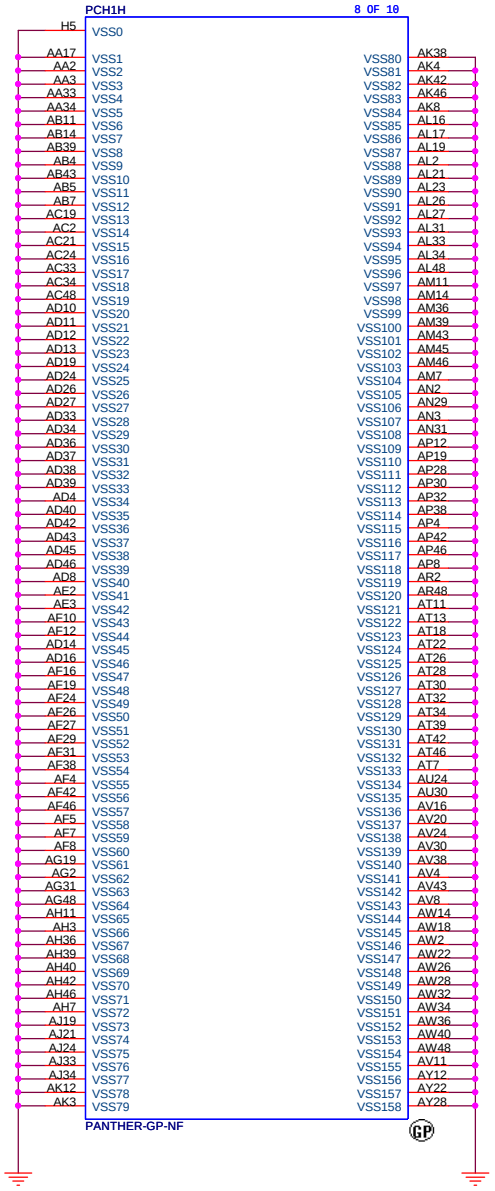
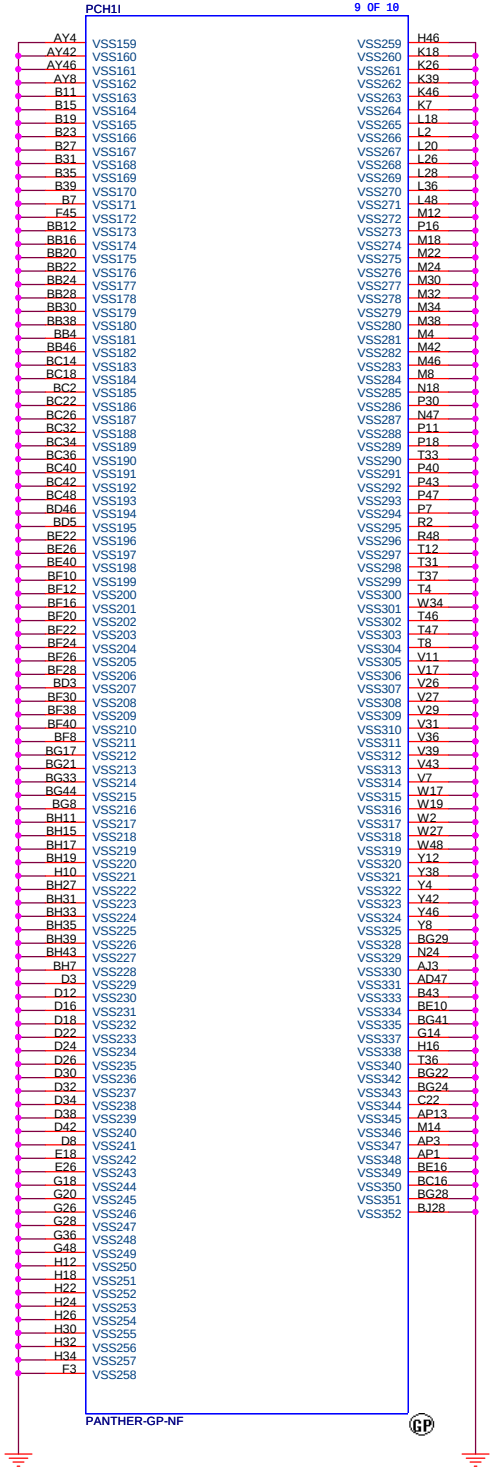
SSID = PCH





JV10-CS

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Title	***PCH (VSS)***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 25 of 103	

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Title	***Reserved***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 26 of 103	

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SSID = KBC

If use PSL function, please connect to 3D3V_AUX_S5
If no use PSL function, please connect 3D3V_AUX_KBC

PCB Version A/D (Pin98)	Pull-Low Resistor	Pull-High Resistor (3D3V_AUX_S5)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.75 V
SC	100.0 K	33.0 K	2.48 V
-1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

65W_90W#
High: 65W / Low 90W

NOTE:
Locate resistors R2719 and R2722 close to the NPCE885P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

71.00885.A0G

R2701 and C2716 Need very close to EC

Prevent BIOS data loss solution

84.T3906.A11
2nd = 84.03906.F11

74.00690.I7B

EC_GPIO47 High Active

84.2N702.J31
2nd = 84.2N702.W31

83.00016.K11
2ND = 83.00016.F11

EC GPIO standard PH/PL

LILI Multi GPIO setting

84.DMN66.03F
2ND = 84.2N702.A3F

MODEL_ID_AD (Pin100)	Pull-Low Register	Pull-High Register	Voltage	
LG48 UMA	100.0 K	10.0 K	3.000 V	64.10025.6DL
LG48 OPTIMUS	100.0 K	20.0 K	2.750 V	64.20025.6DL
LG58 UMA	100.0 K	33.0 K	2.481 V	64.33025.6DL
LG58 OPTIMUS	100.0 K	47.0 K	2.245 V	64.47025.6DL

64.47025.6DL

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795
Size: Document Number: G48/G58 Rev: SC
Date: Friday, February 17, 2012 Sheet 27 of 103

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SSID = Thermal

Thermal sensor

Close to PCH on top side.

SA_0905_change to 390p

3 Q6 MMBT3904WT1G-GP — C183 SC390P50V2KX-GP

2 Q42 MMBT3904WT1G-GP — C434 SC390P50V2KX-GP (DY) (DY)

2200p close to smsc2103 chip

REMOTE2- — C569 SC2200P50V2KX-2GP — REMOTE2+

between CPU, VGA and DIMM on bottom side

T8

1 Q9 MMBT3904WT1G-GP

2200p close to smsc2103 chip

H_THERMDA — C389 SC2200P50V2KX-2GP — H_THERMDC

CPU backside or inside the socket

CPU TEMP:
H_THERMDA and H_THERMDC routing 10mil trace width
and spacing. Locate Capacity near Thermal diode.

T8= 86 degree

3D3V_S0 — R2803 6K8R2J-GP — THERM_SYS_SHDN#

3D3V_S0 — R2802 15KR2J-1-GP — THERM_SCI#

3D3V_S0 — R260 68R2-GP — C388 SCD1U10V2KX-4GP — 2103_VDD

U2801 EMC1423-1-AIZL-TR-GP

1	VDD	SMCLK	10
2	DP1	SMDATA	9
3	DN1	ALERT#	8
4	DP2/DN3	SYS_SHDN#	7
5	DN2/DP3	GND	6

H_THERMDA
H_THERMDC
REMOTE2+
REMOTE2-

SMBC_THERM 27,86
SMBD_THERM 27,86
THERM_SCI#
THERM_SYS_SHDN#
R272 0R2J-2-GP
THERM_SCI#

4 WIRE PWM Fan Control circuit

5V_S0

Close to connector

D2801 CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
DY
C39 SC47U6D3VKX-GP

R426 10KR2J-3-GP
R2801 0R3J-0-U-GP
R427 0R0402-PAD SIT

27 FAN_PWM — FAN_PWM — FAN_PWM_C
27 FAN_TACH — FAN_TACH
5V_S0_FAN

FAN1

EC2801 SC470P50V2JN-GP SIT
EC2802 SC470P50V2JN-GP
ACES-CON4-GP-U1

20.F0714.004
2nd = 20.D0196.104

TP2803 TP2802 TP2801 AFTP2804 — FAN_PWM_C, FAN_TACH, 5V_S0_FAN

3D3V_AUX_S5

D2803 BAT54PT-GP
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.BAT54.S81
DY

27,36,86 PURE_HW_SHUTDOWN#

Q2802 2N7002K-2-GP
S — THERM_SYS_SHDN#
G — IMVP_PWRGD_T
D

3D3V_S0 — DY R2809 100KR2J-1-GP — SIV

3D3V_S0 — R2810 0R2J-2-GP — DY R2811 0R2J-2-GP — IMVP_PWRGD 36,42

3D3V_S0 — R2814 10KR2J-3-GP SIT

JV10-CS

DY R2812 10KR2J-3-GP

DY C2811 SCD1U10V2KX-5GP

84.2N702.J31
2ND = 84.2N702.W31

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	THERMAL EMC1423		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 28 of 103		

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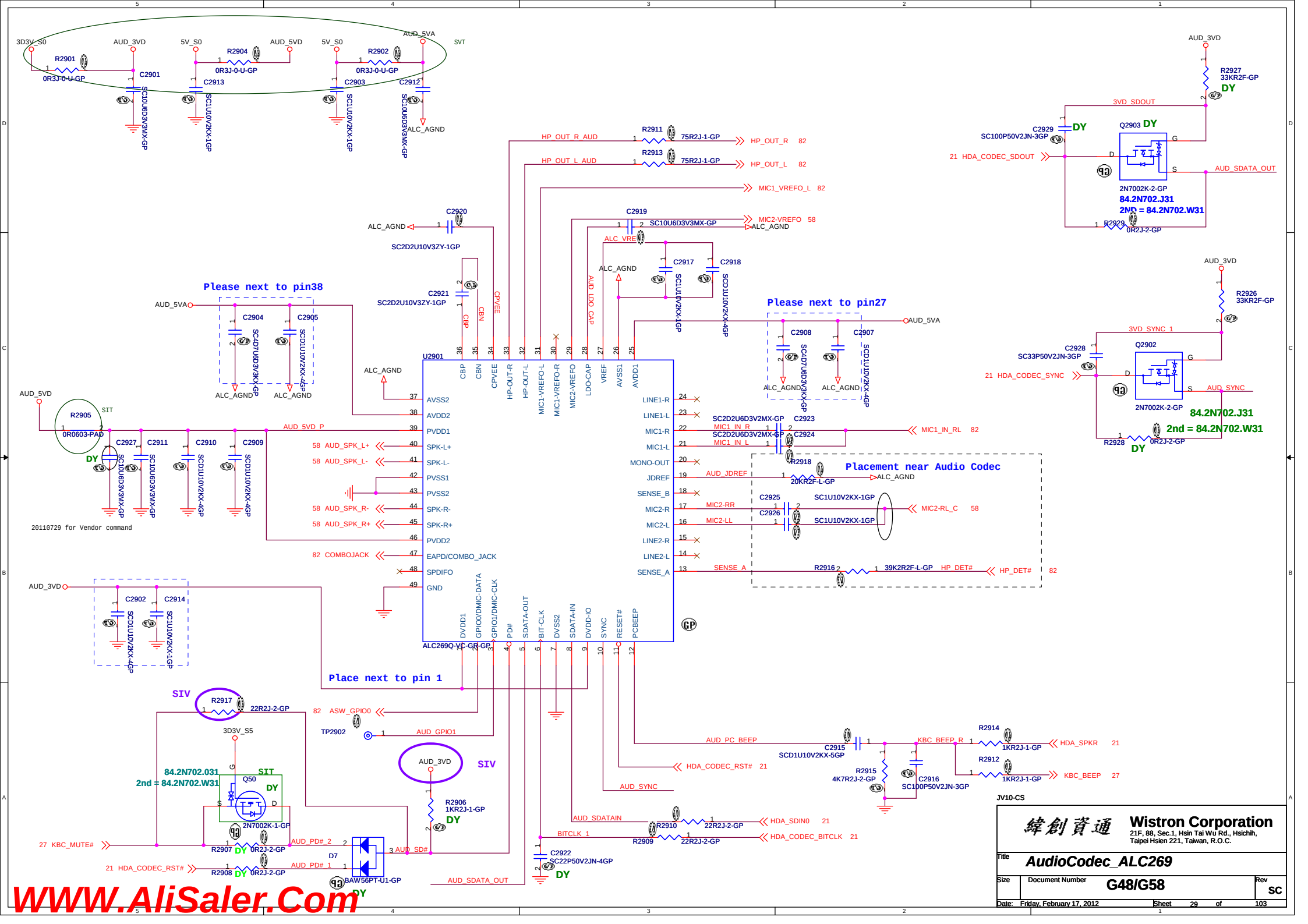

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(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Audio_AMP	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 30 of 103	

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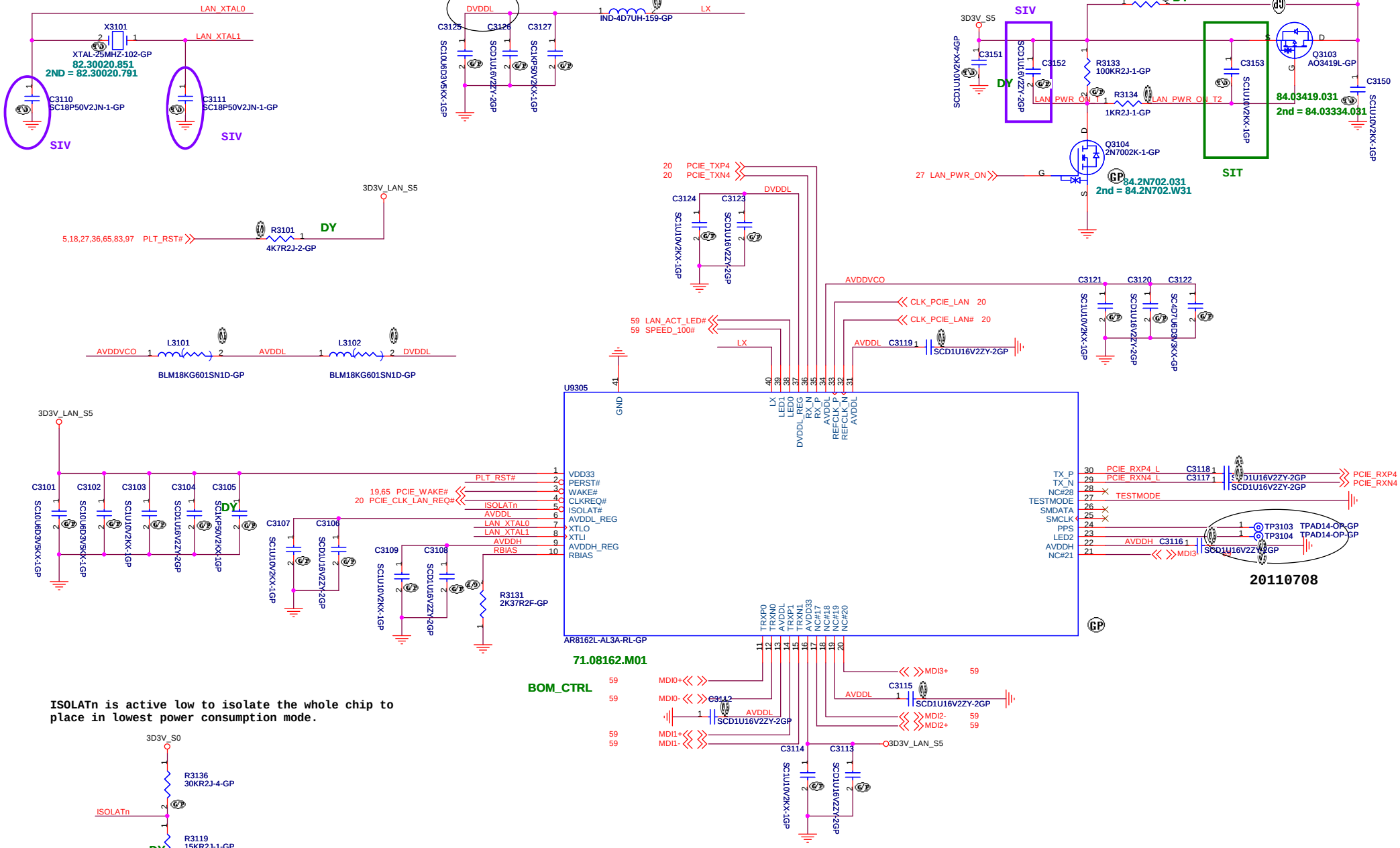
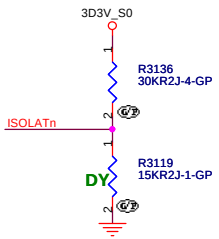
25MHz XTAL



ISOLATn is active low to isolate the whole chip to place in lowest power consumption mode.



JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LOM		
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 31 of 103		

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(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Card reader	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 32 of 103	

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(Blanking)

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1394		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012		Sheet 33 of	103

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(Blanking)

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Smart card	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 34 of 103	

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Reserved

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB 3.0 CONTROLLER***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 35 of 103	

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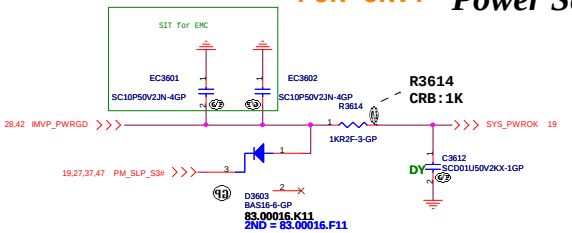
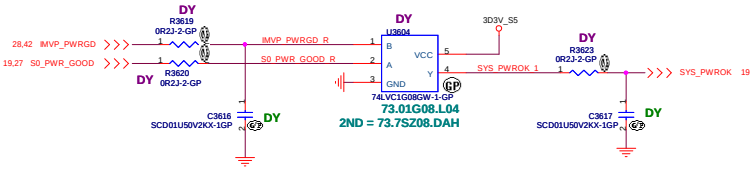
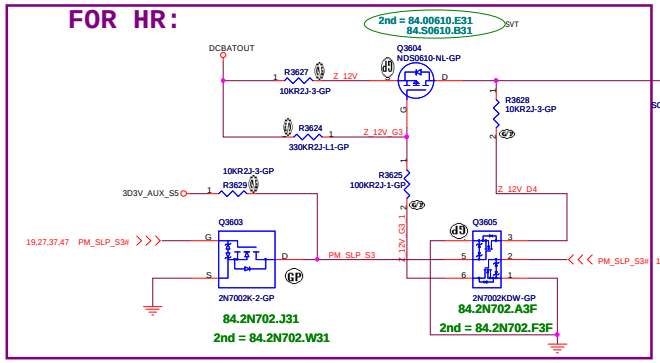
FOR CRV: Power Sequence

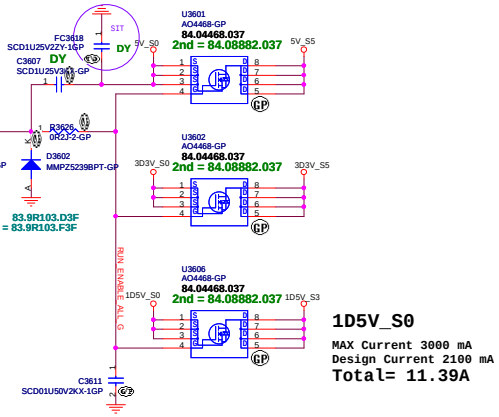


FOR HR:



FOR HR:

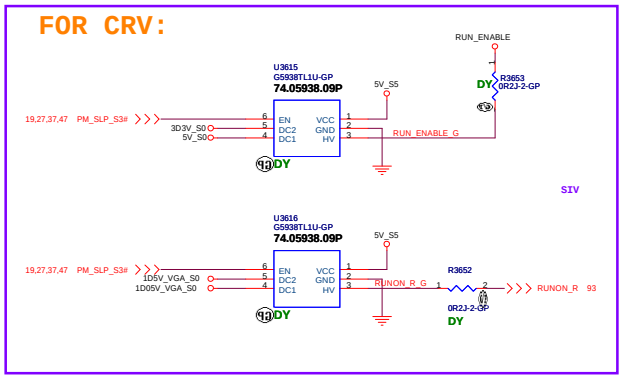


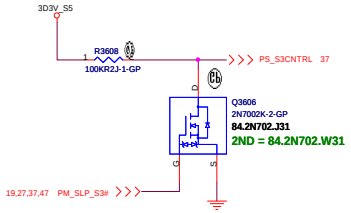


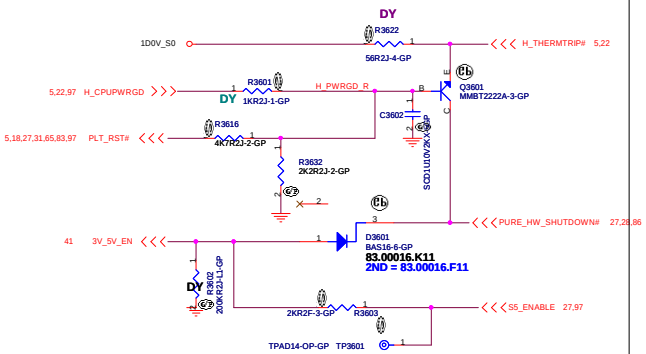
1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

FOR CRV:







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JV10-CS

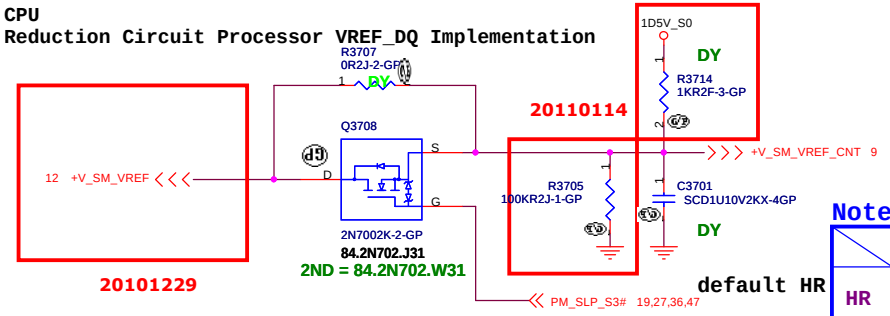
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PowerPlane Enable&Sequence

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 36 of 103

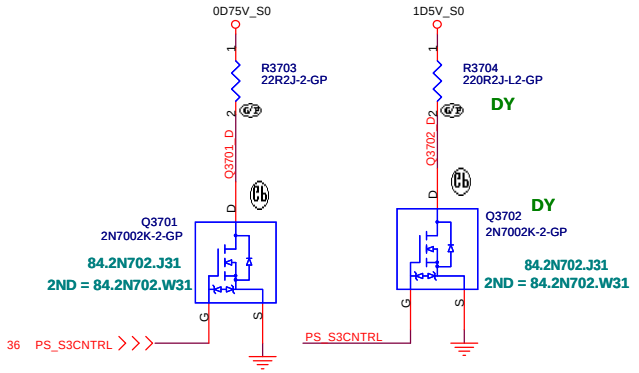
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



Note

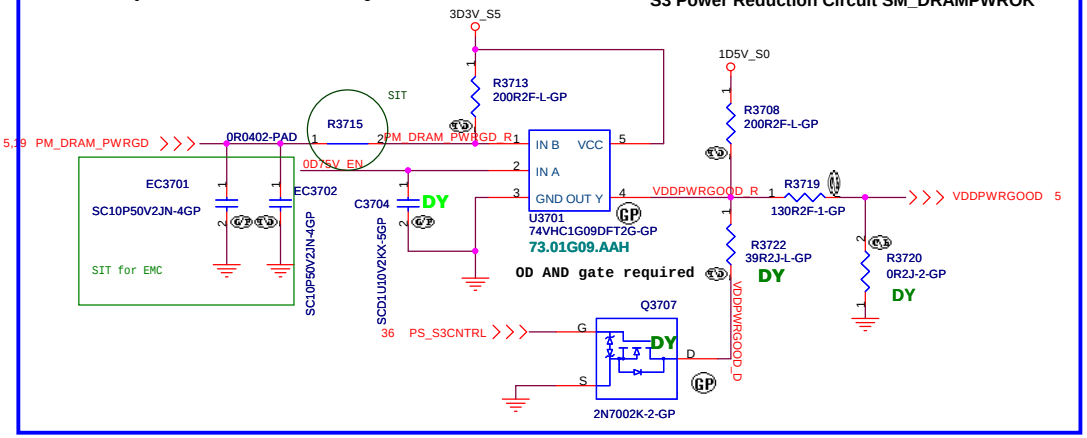
	R3705
HR	100K ohm 63.10434.1DL
CRV	1K ohm 64.10015.6DL

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



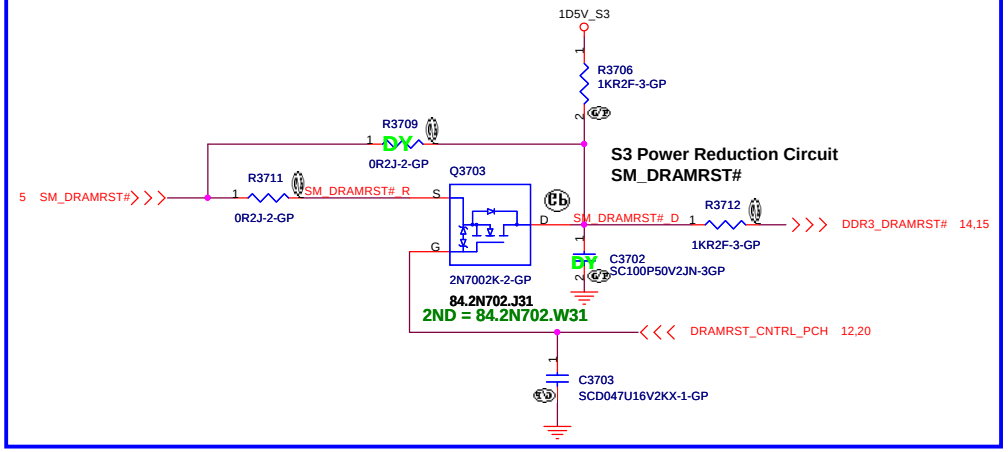
SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

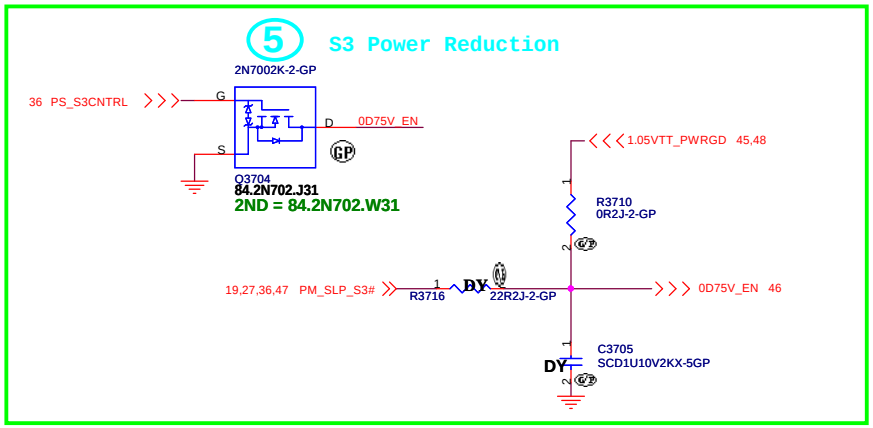


84.2N702.J31
2nd = 84.2N702.W31

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



5 S3 Power Reduction



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ADAPTER OCP / S3 reduction	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 37 of 103	

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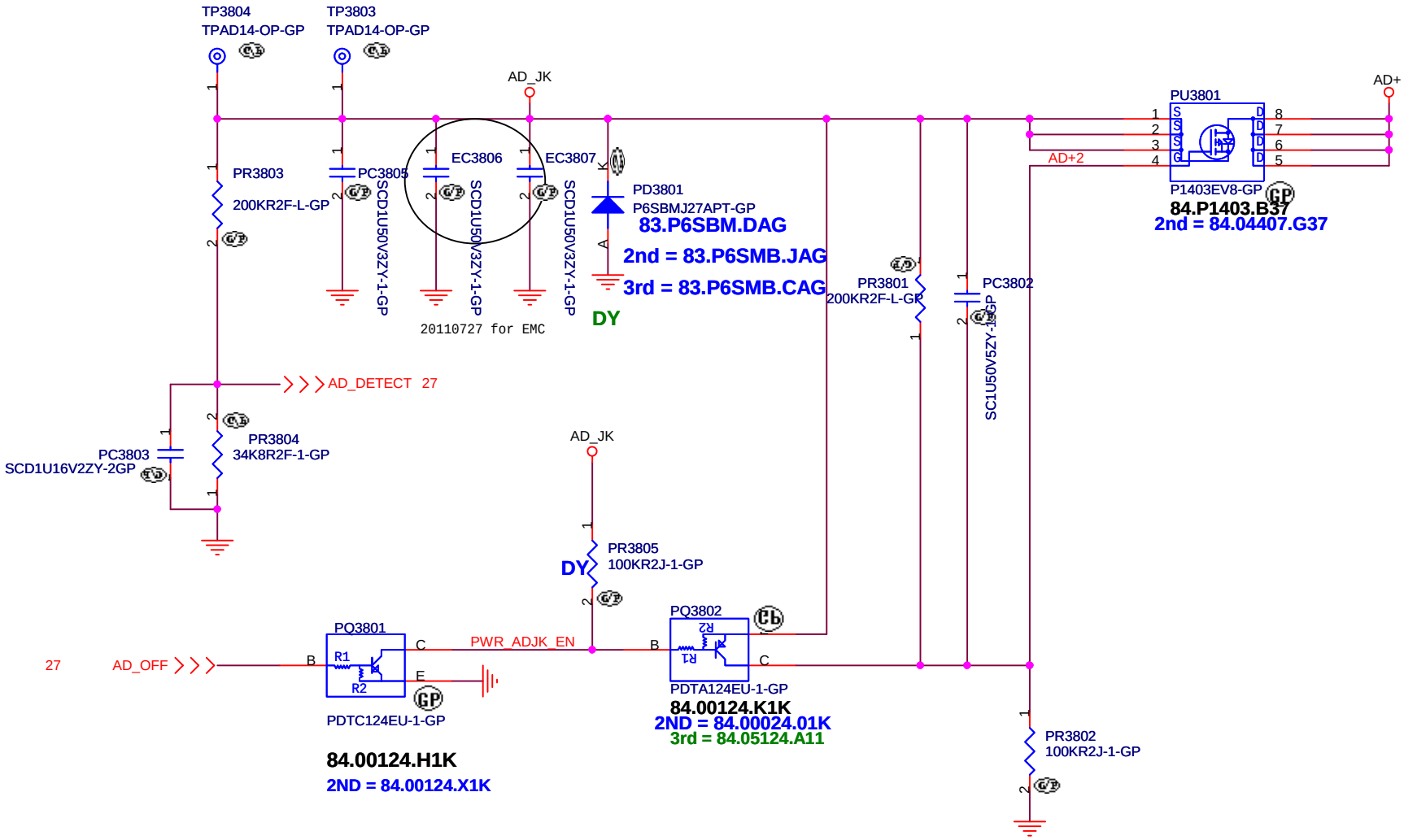
Adaptor in to generate DCBATOUT



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN JACK***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 38 of 103	

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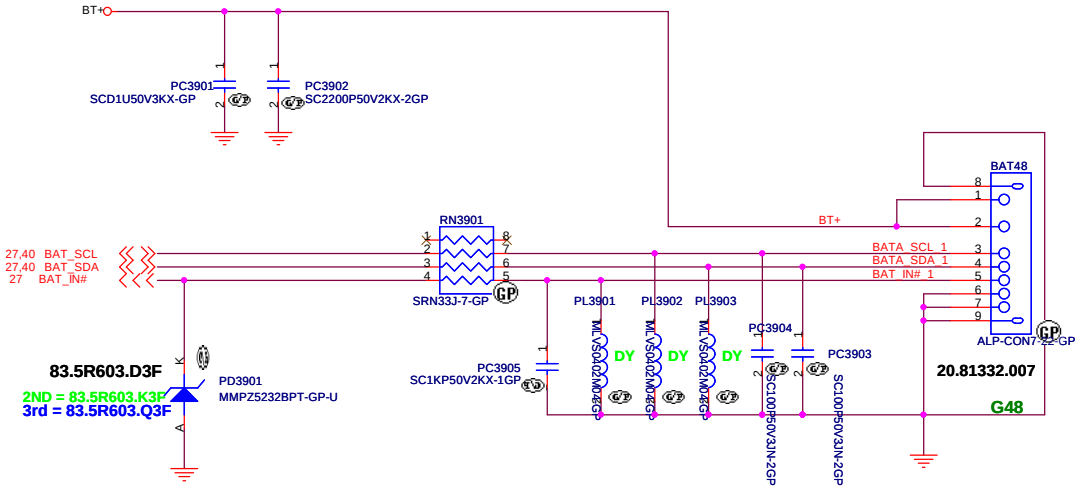
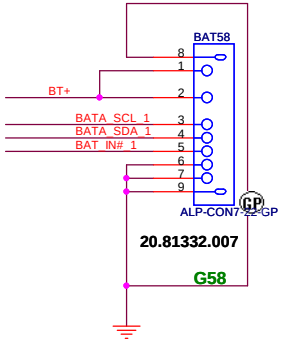
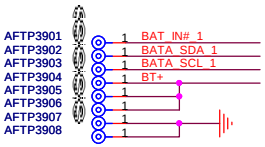
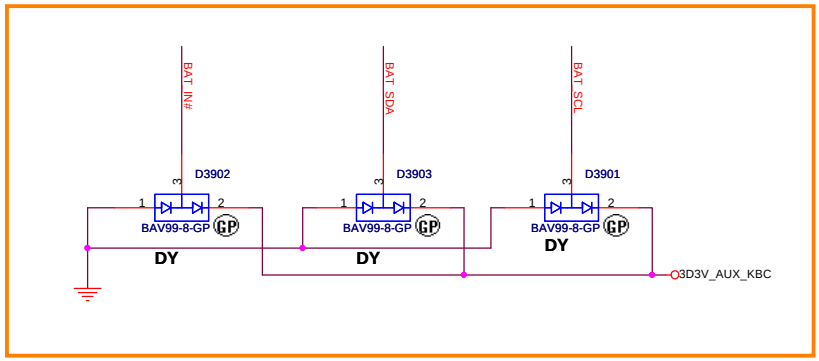
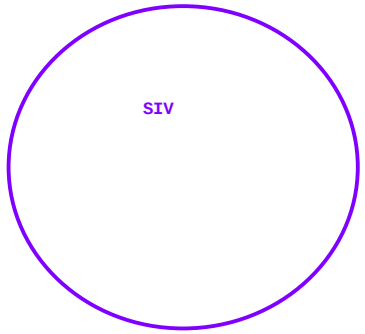
BATTERY CONNECTOR











JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT CONN		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 39 of 103	

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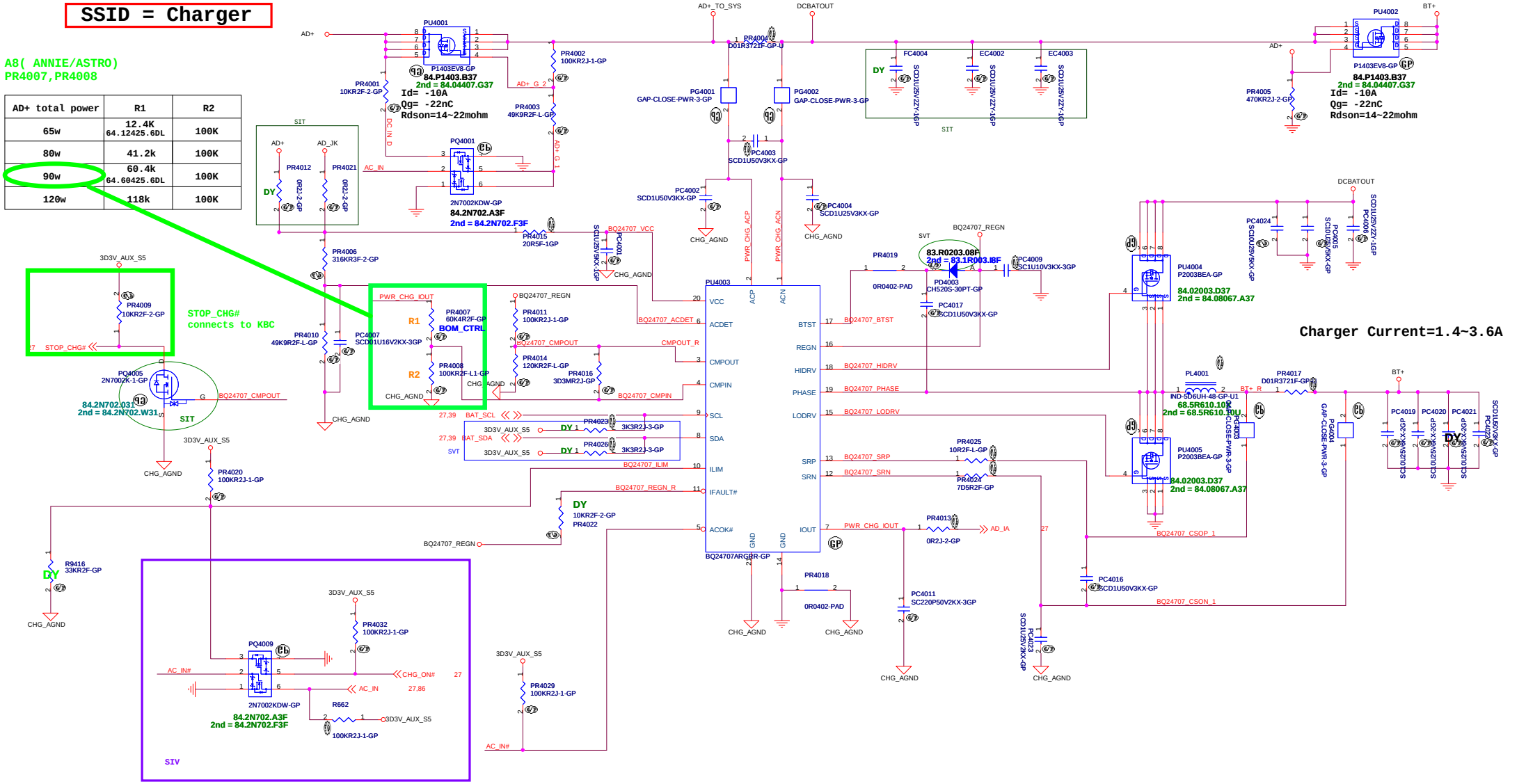
SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	12.4K 64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k 64.60425.6DL	100K
120w	118k	100K



JV10-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BQ24745_Charger

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 40 of 103

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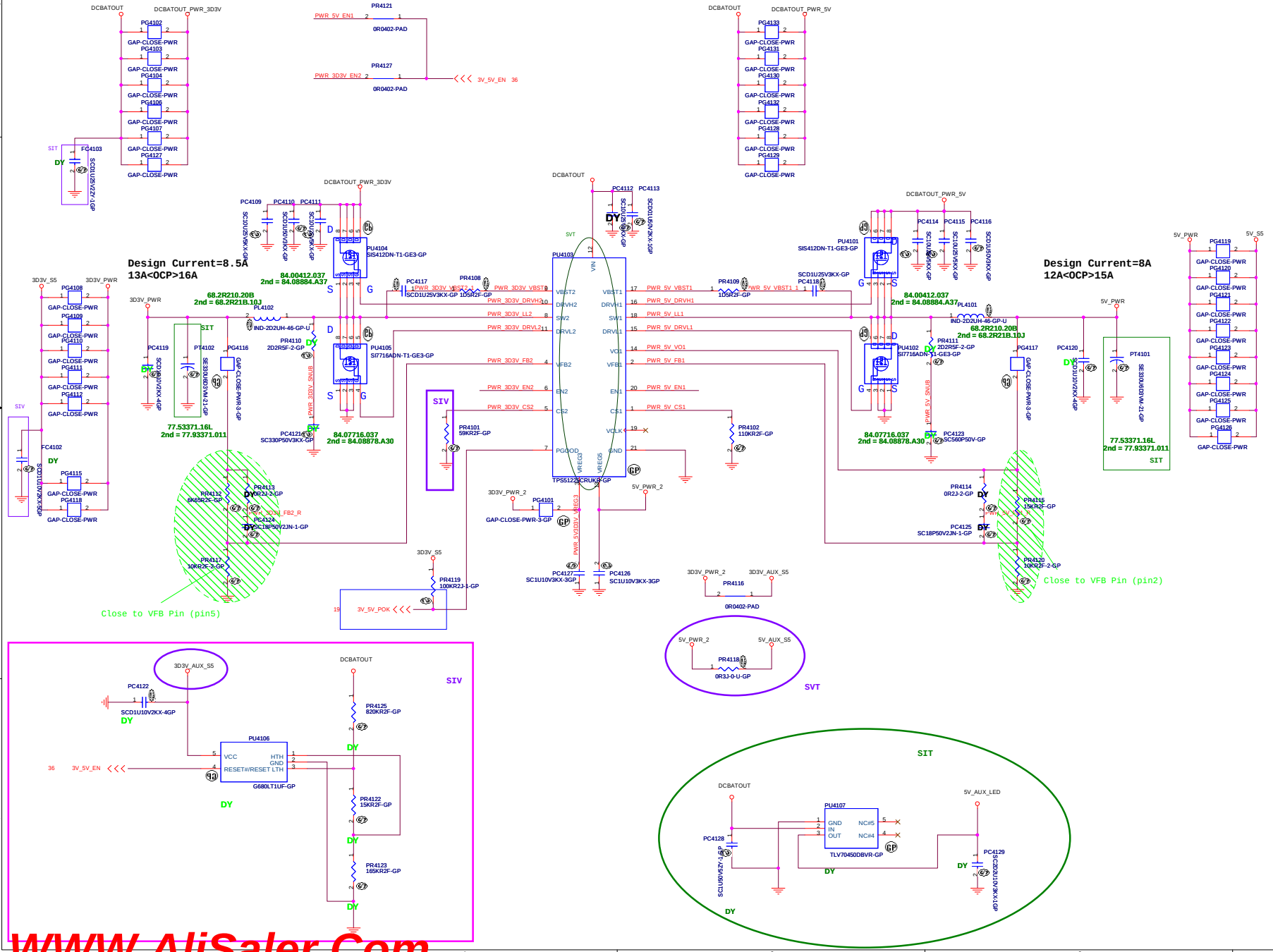
SSID = PWR.Plane.Regulator_5v3p3v



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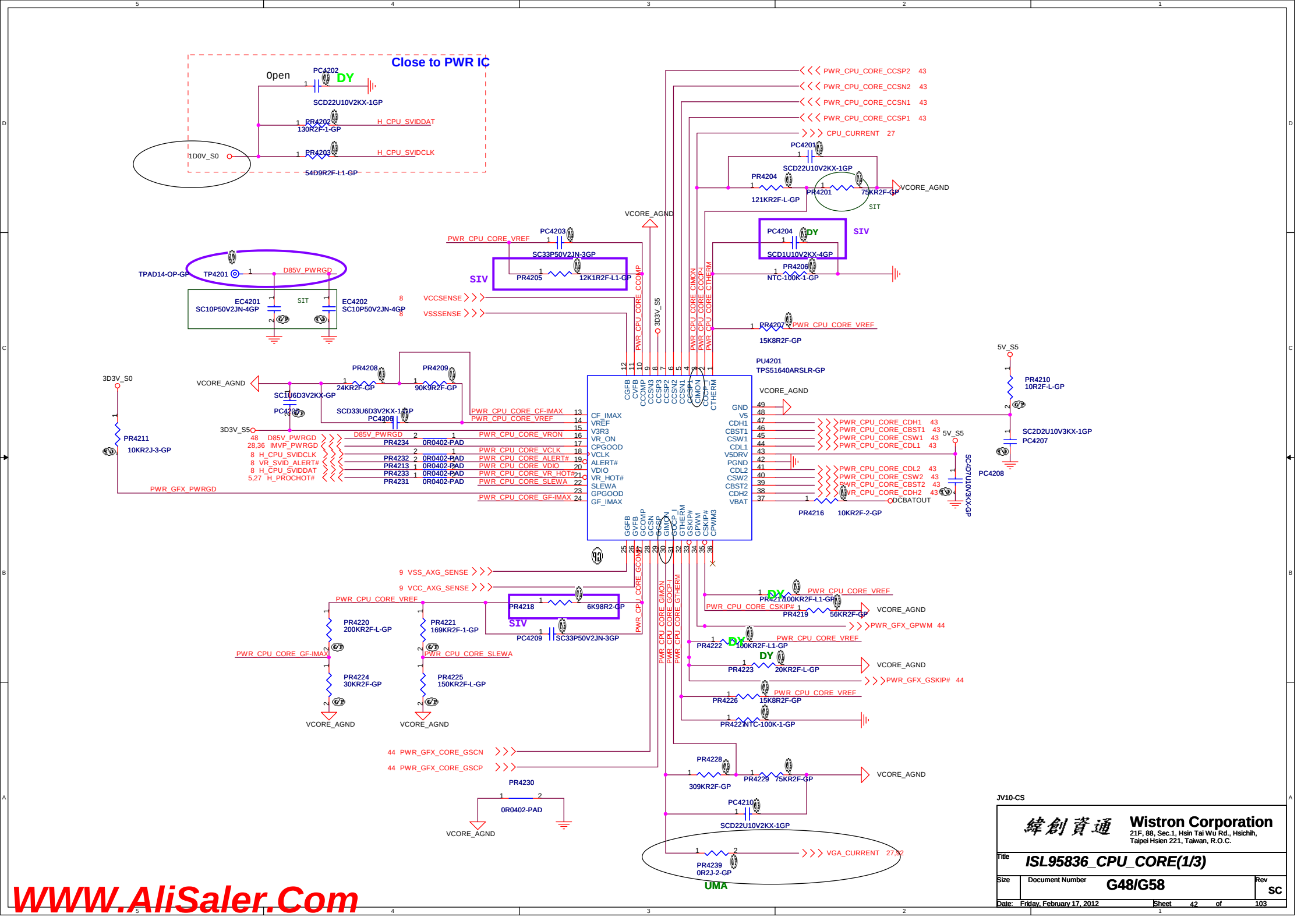
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51123_5V_3D3V	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 41 of 103	



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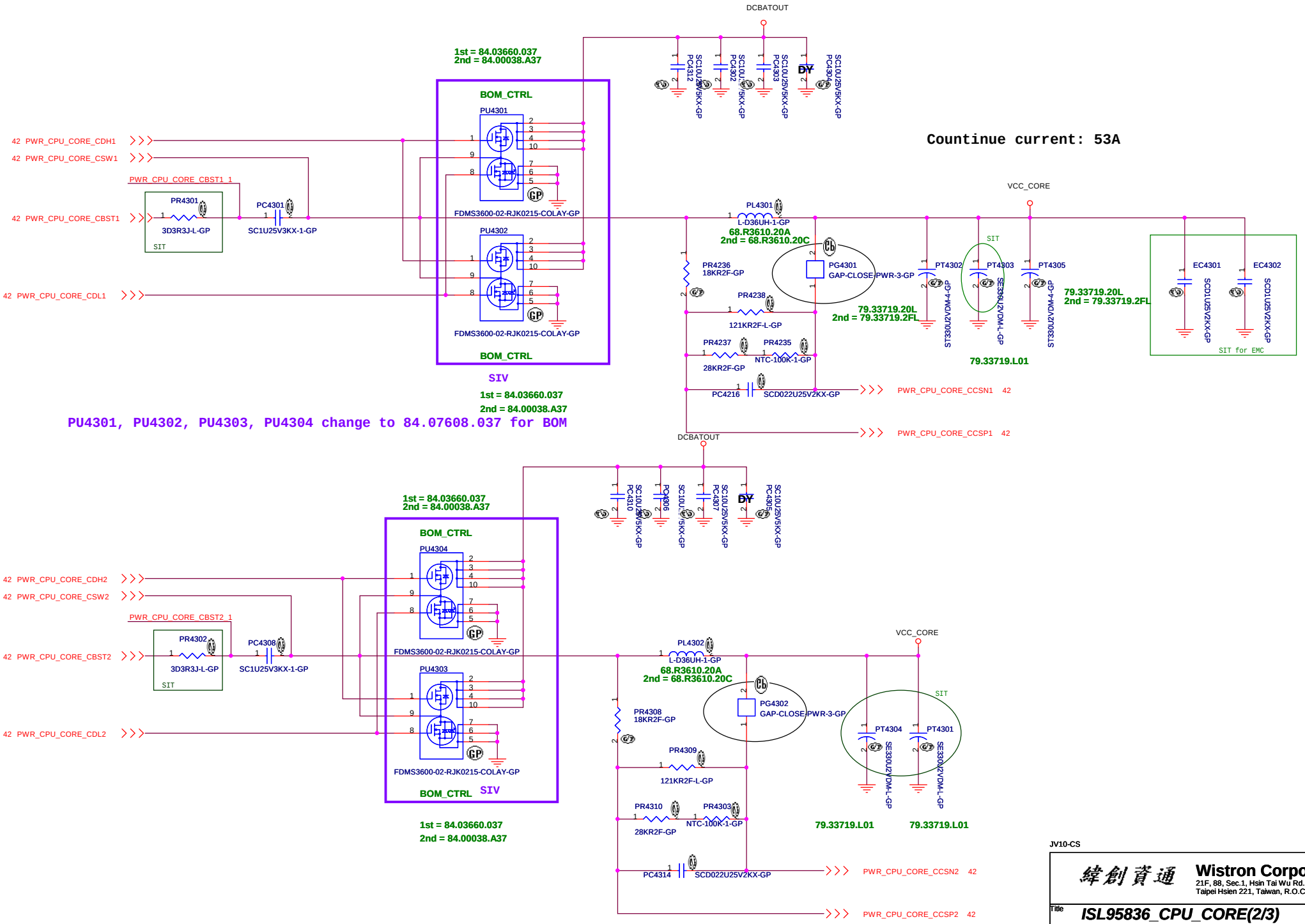

PU4301, PU4302, PU4303, PU4304 change to 84.07608.037 for BOM

JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL95836_CPU_CORE(2/3)	
Size	Document Number G48/G58	Rev SC
Date: Monday, February 20, 2012	Sheet 43 of 103	

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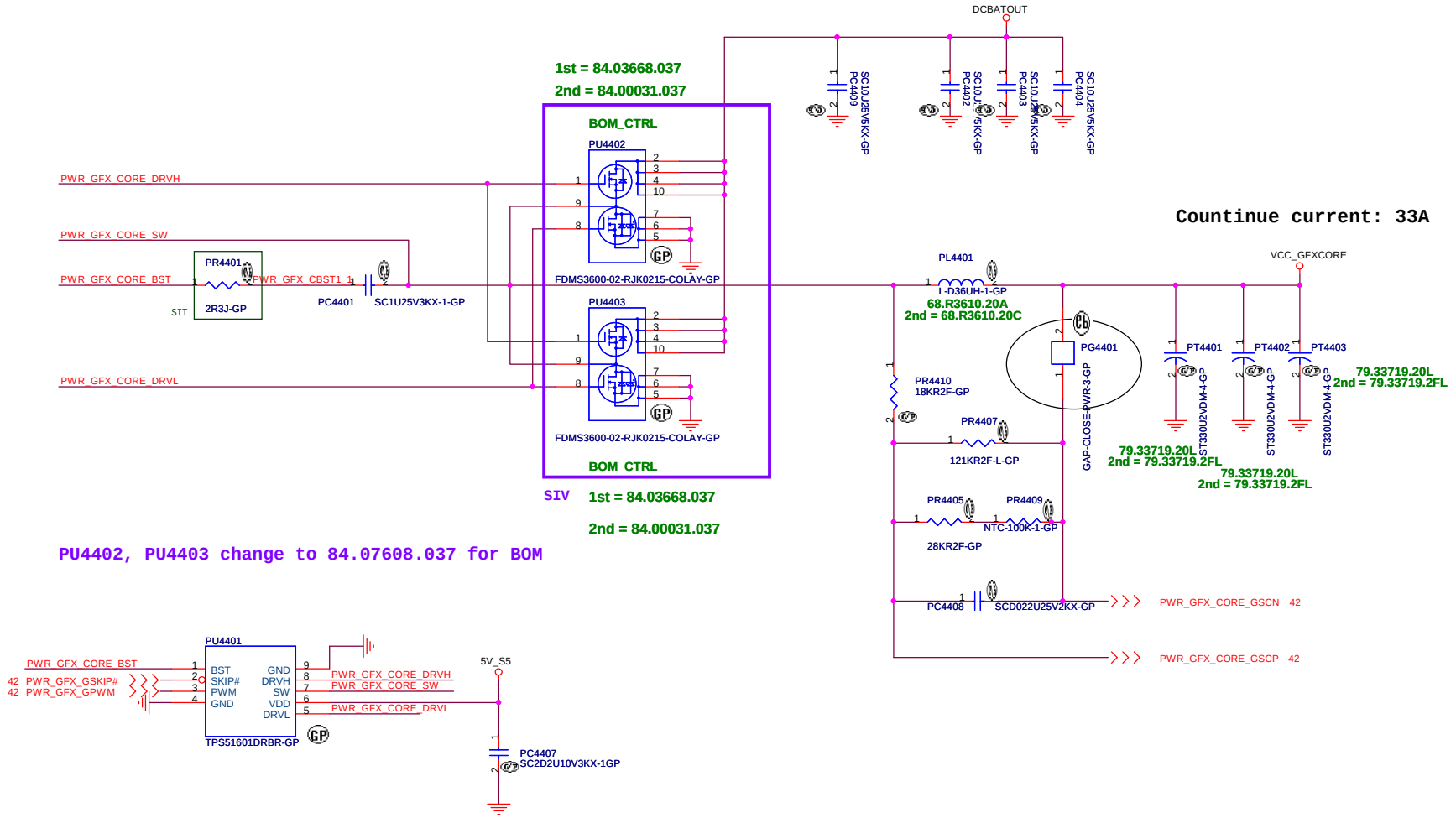

JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ISL95836_CPU_CORE(3/3)		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 44 of 103	

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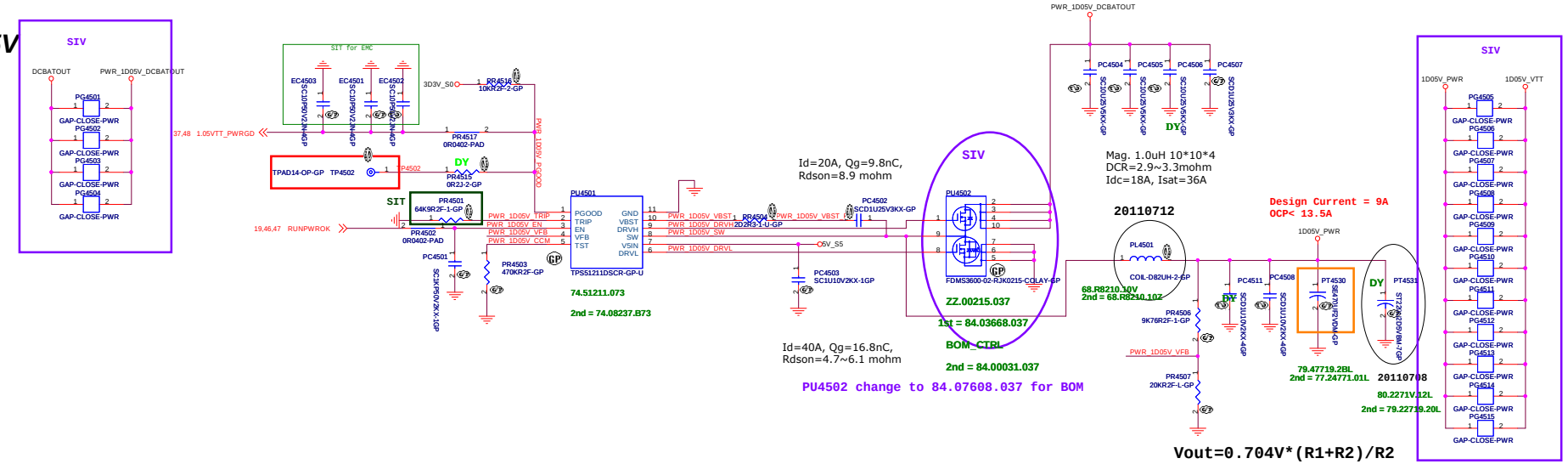
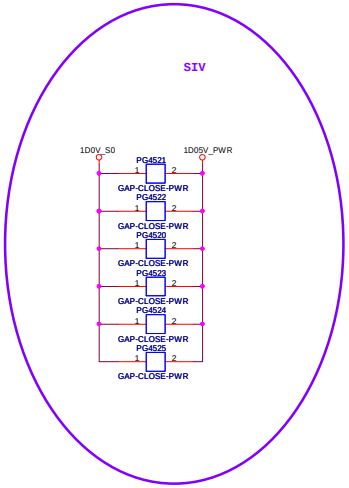
TPS51211 for 1D05V



APL5916 for 1D0V



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS51211_1D05V&TPS51219_1D0V		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 45 of 103	

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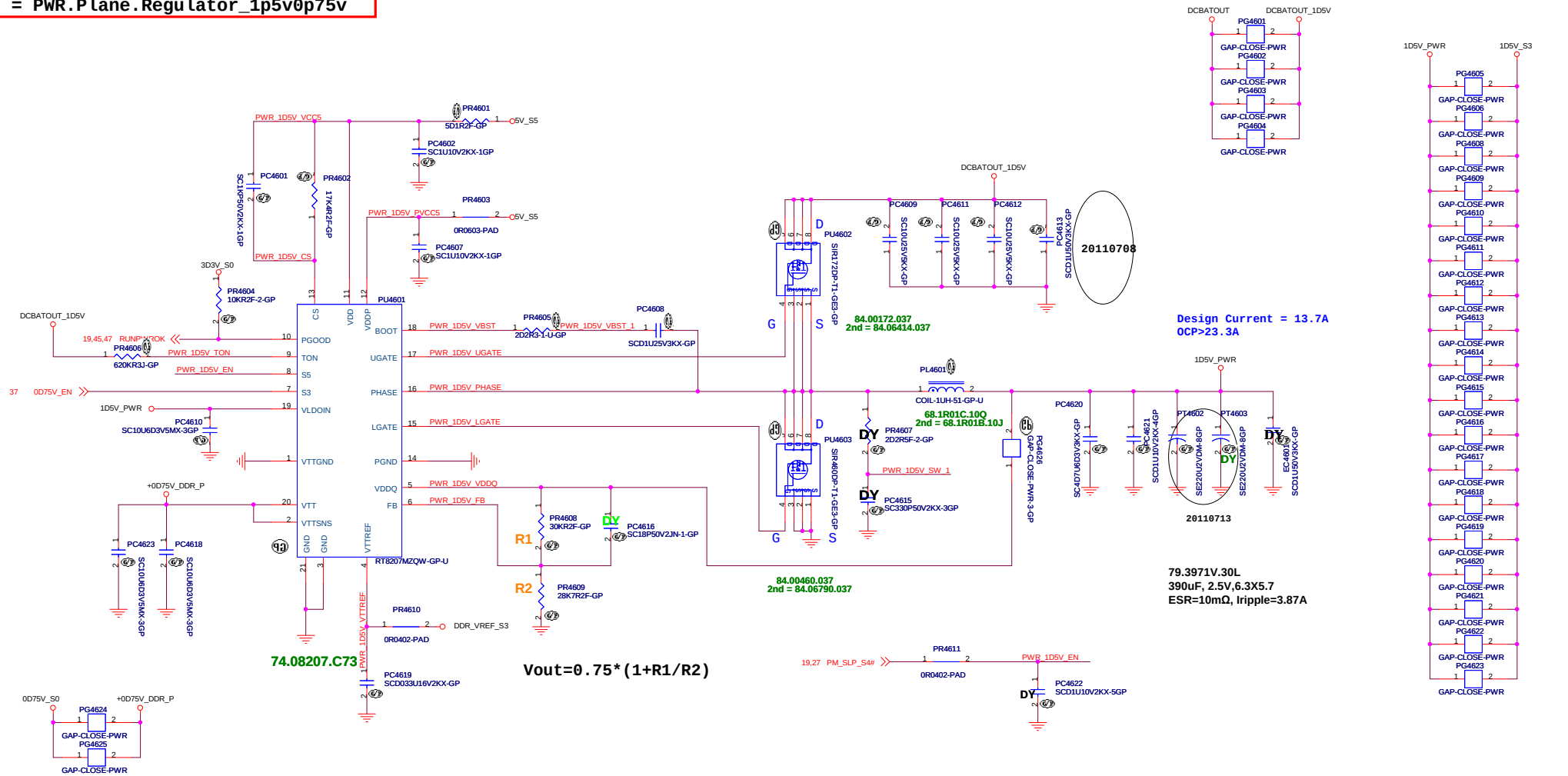
SSID = PWR.Plane.Regulator_1p5v0p75v



JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8207_1D5V_0D75V		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 46 of 103	

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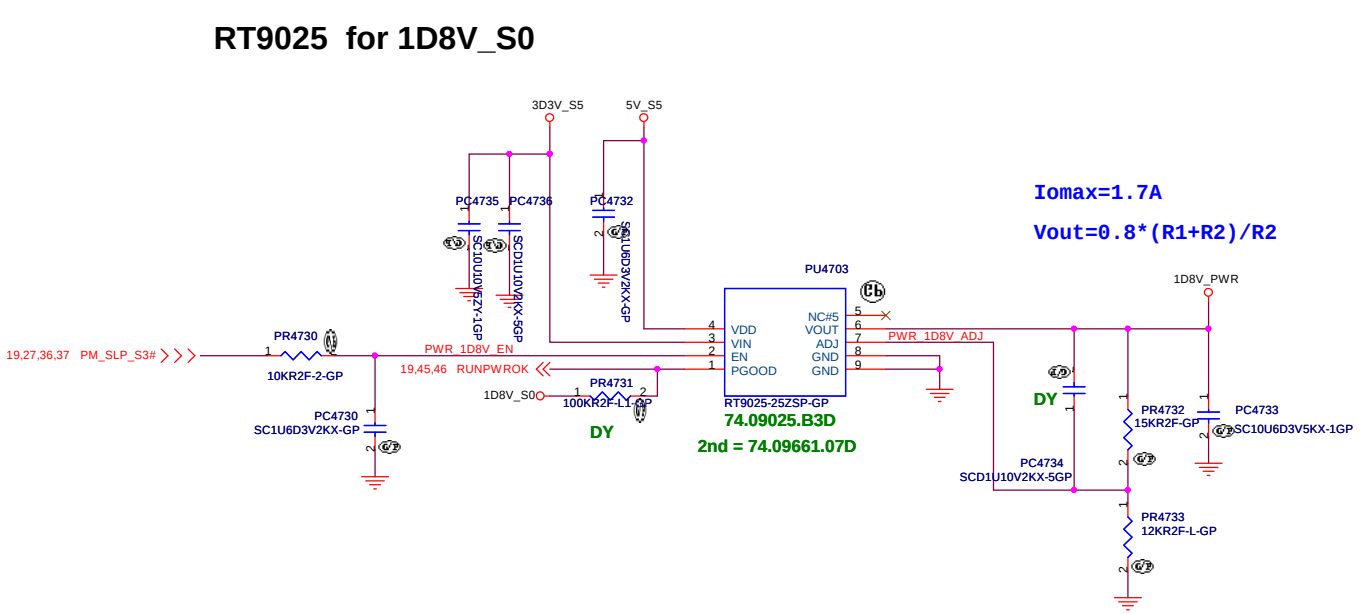
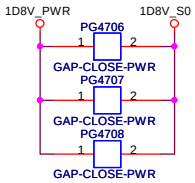
RT9025 for 1D8V_S0





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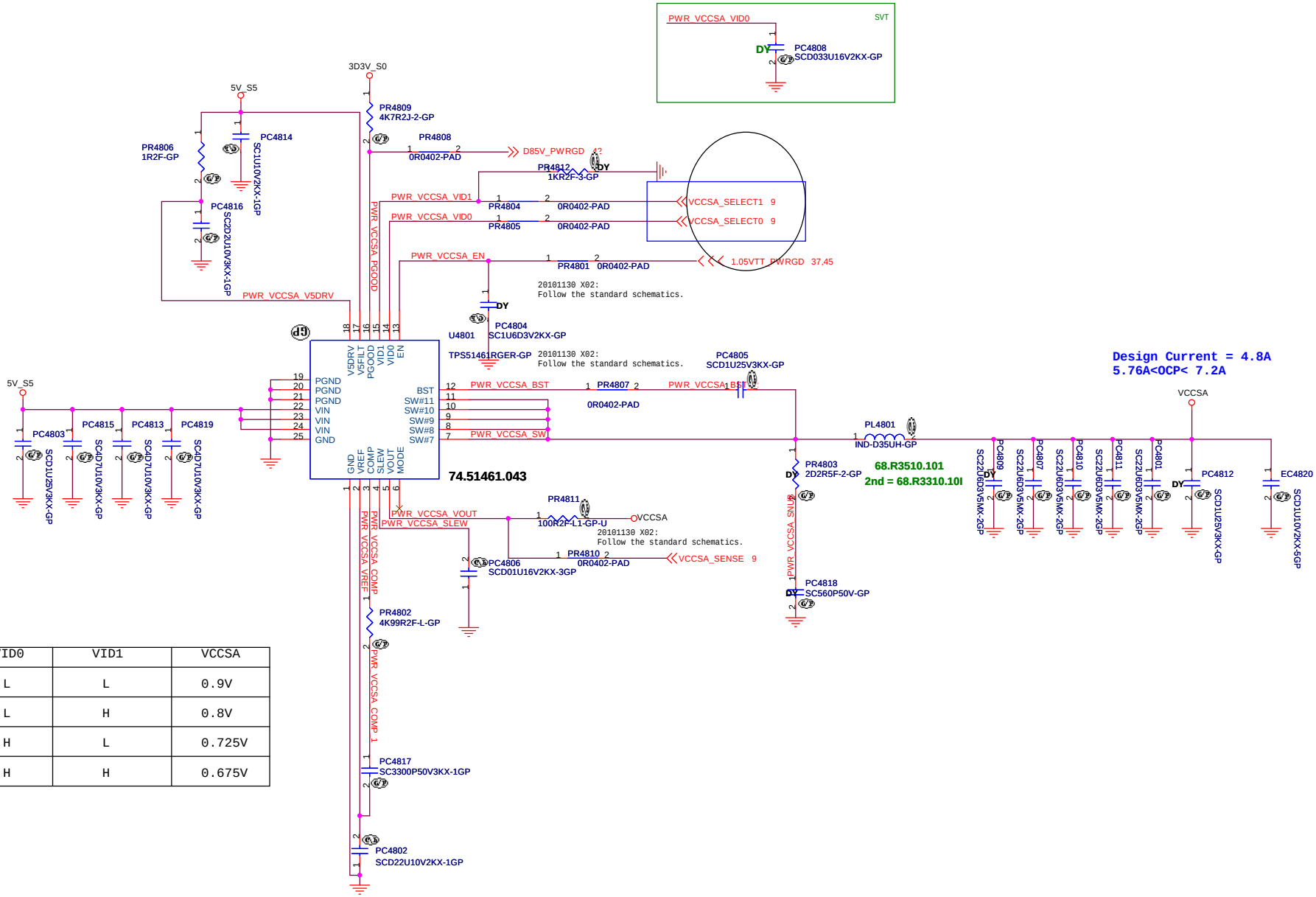
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT9205_1D8V	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

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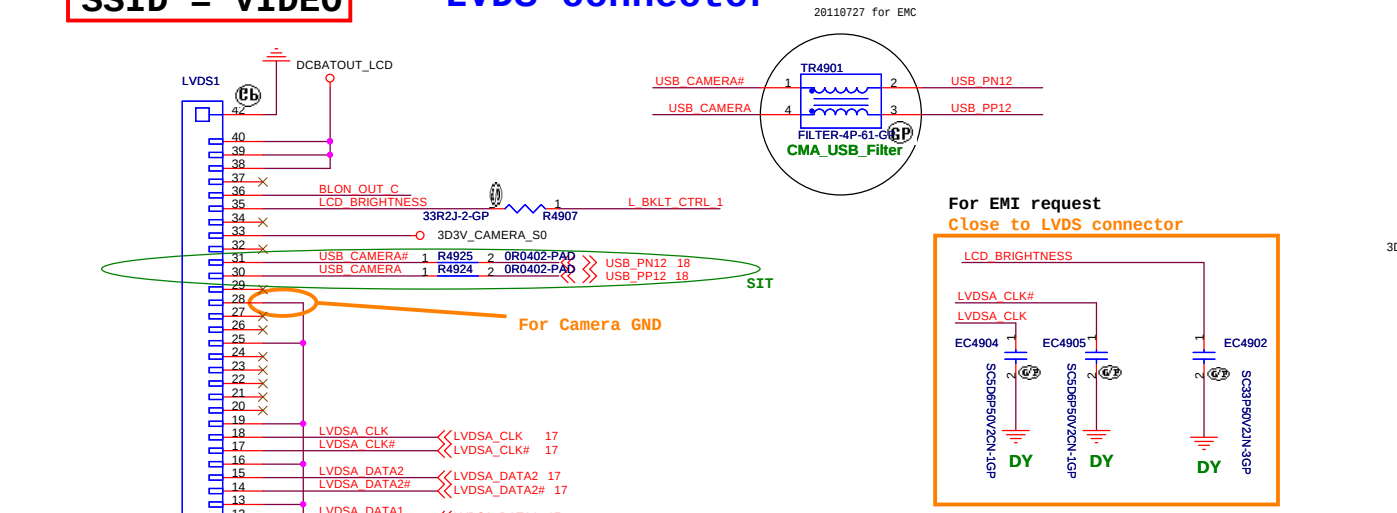
JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA_TPS51461	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 48 of 103	

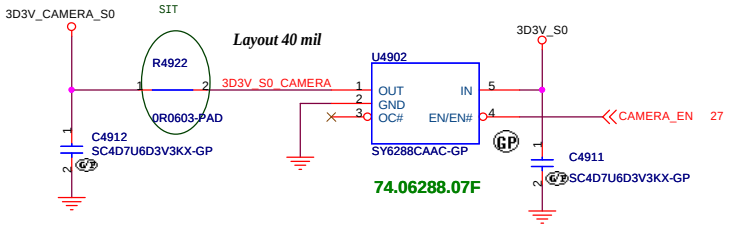
SSID = VIDEO

LVDS connector



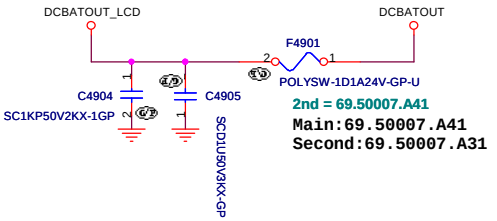
For EMI request
Close to LVDS connector

CAMERA POWER

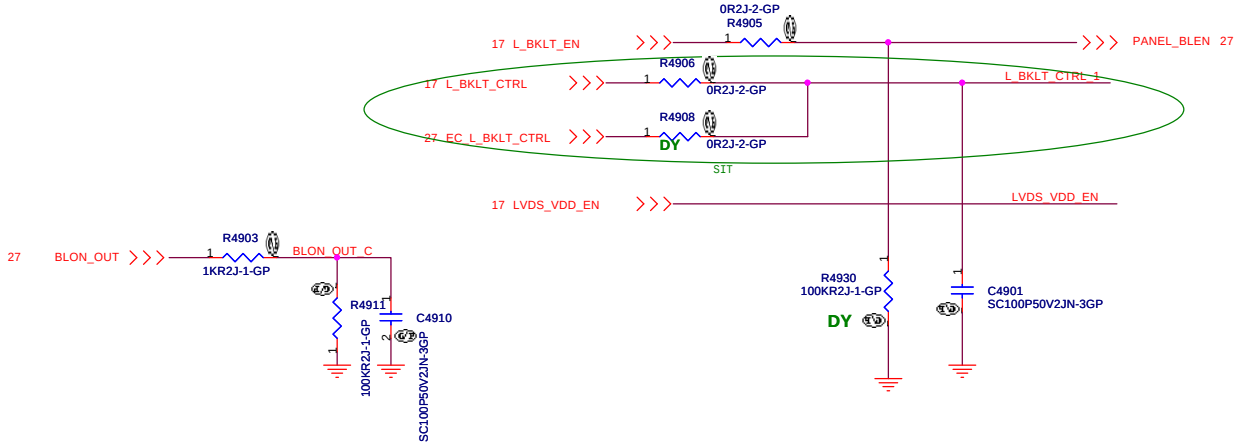


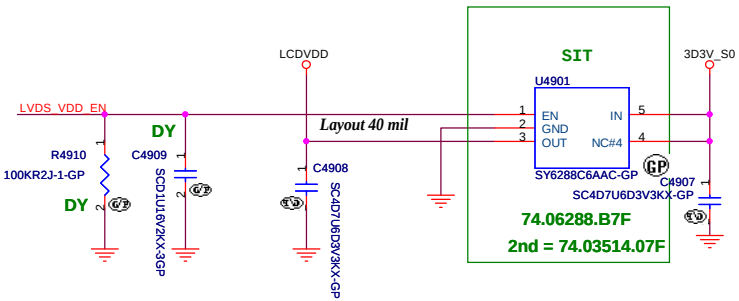
U4902 Change to 74.07534 from 74.05240.A7F for obsoleted part

LCD POWER



Panel BL brightness/Power En/BL En





JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD/Inverter Connector	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 49 of 103	

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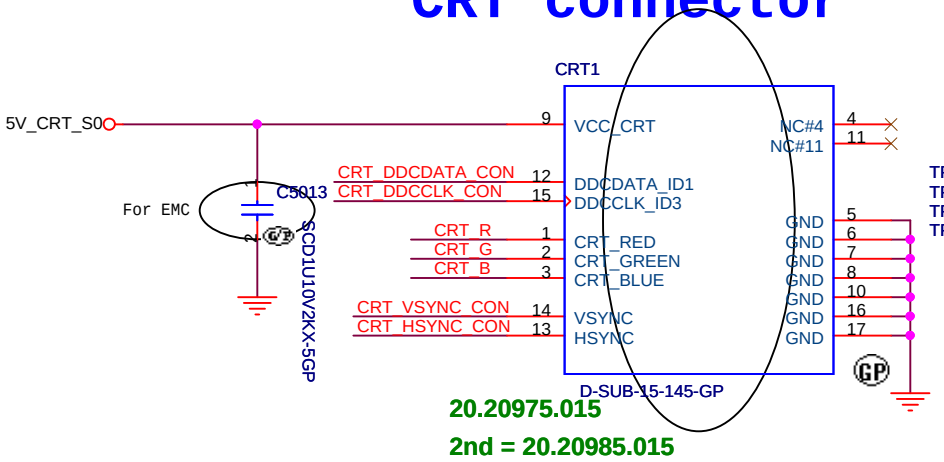
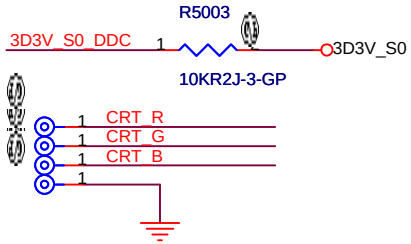
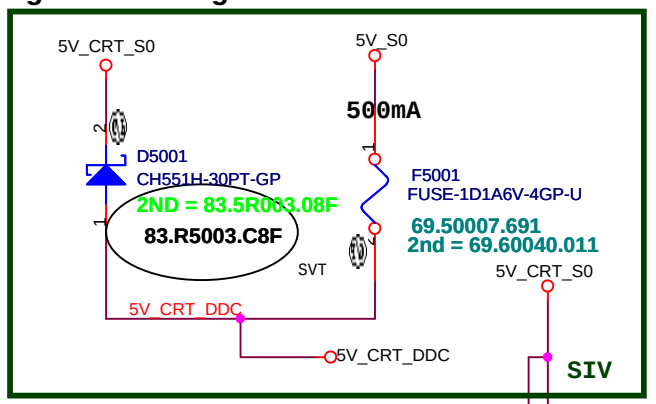
CRT connector



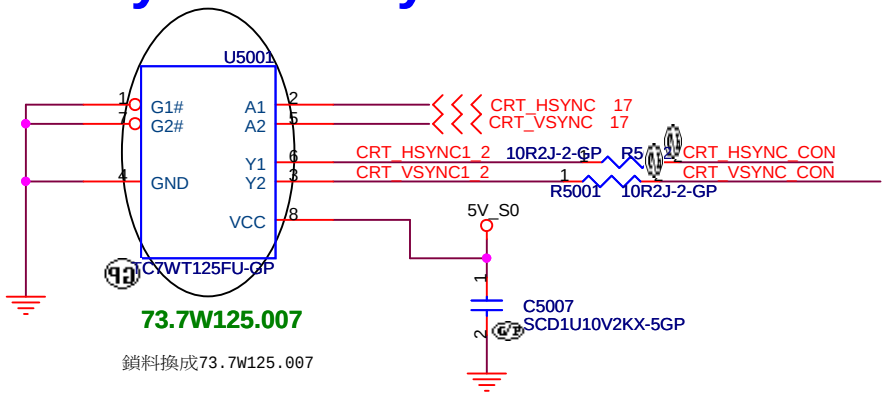


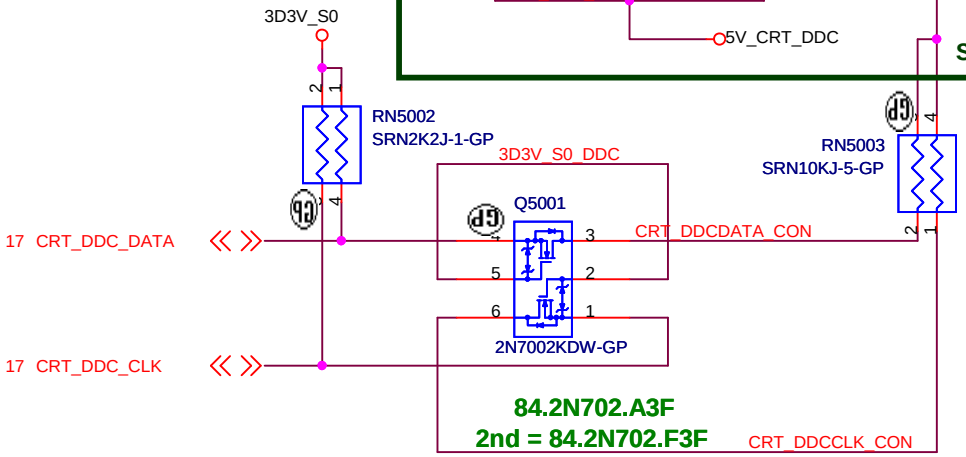
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board



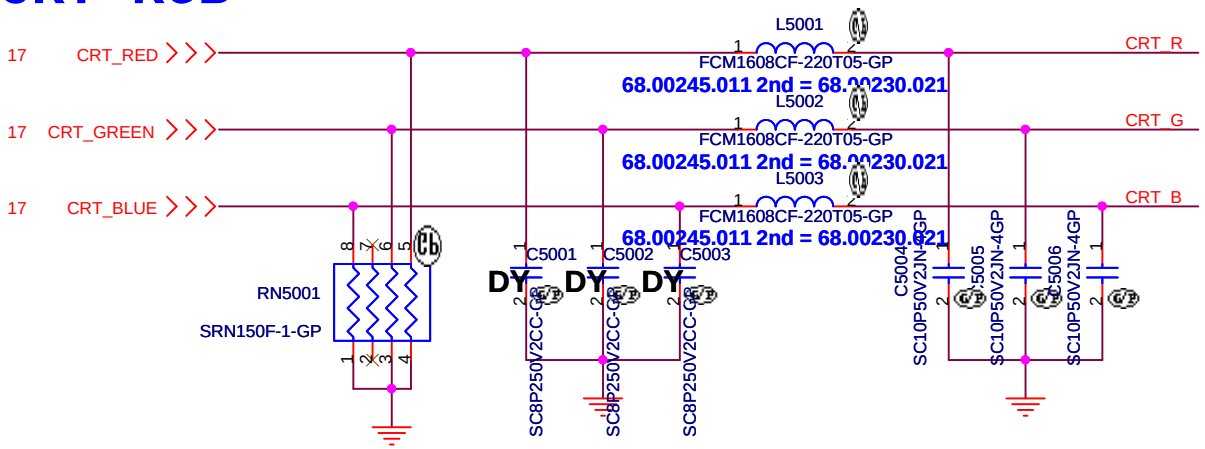
CRT Hsync & Vsync level shift

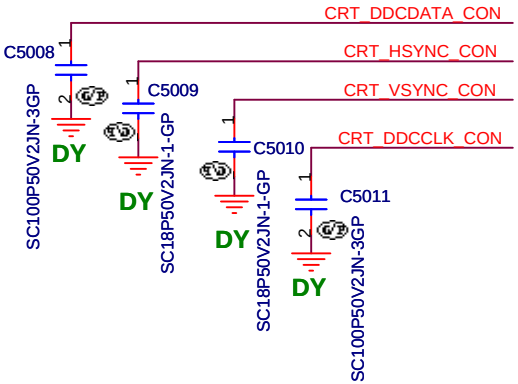




CRT RGB

R,G,B place 22pF and ESD diode for intel check list





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Title	CRT Board Connector	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 50 of 103	

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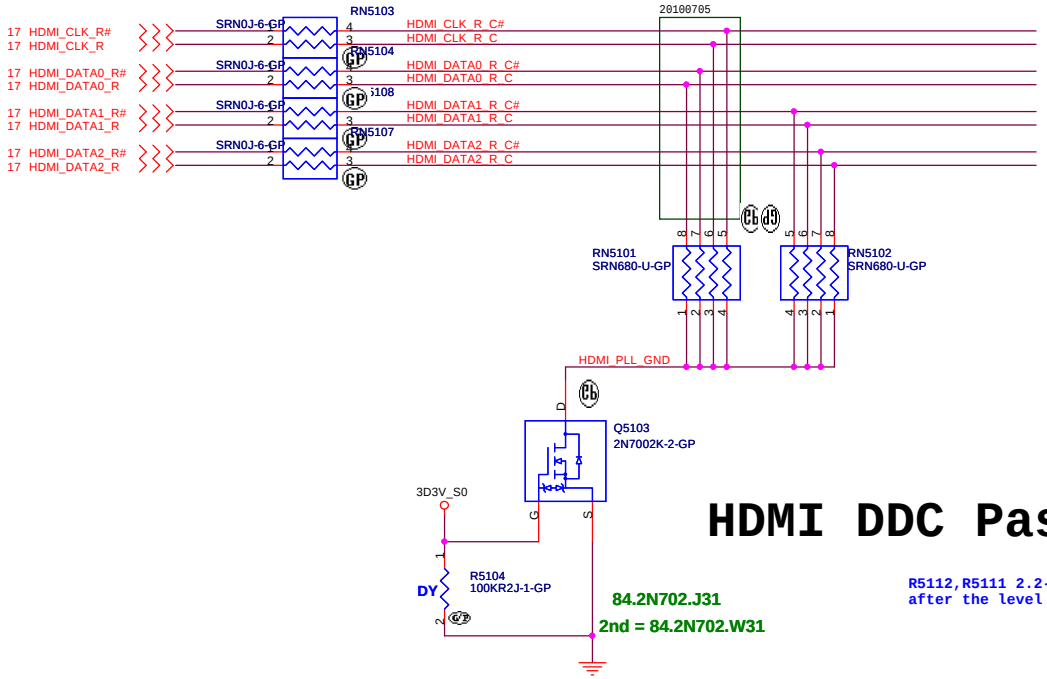
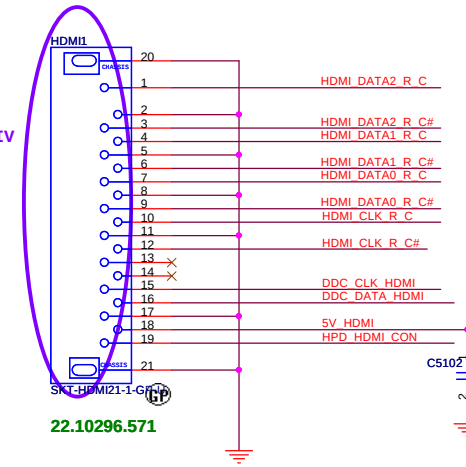
SSID = VIDEO

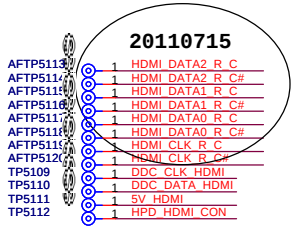
HDMI CONNECTOR

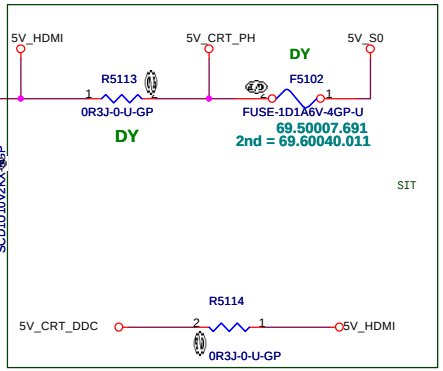
HDMI Passive Level Shifter

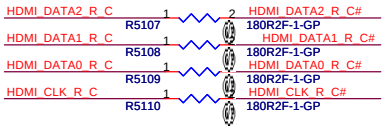
Close to HDMI Connector





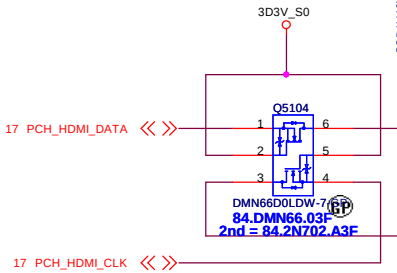


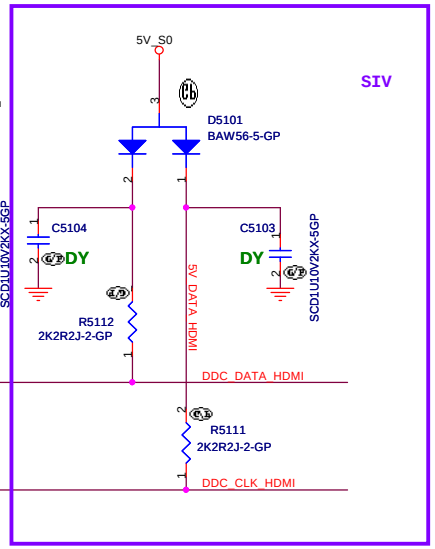


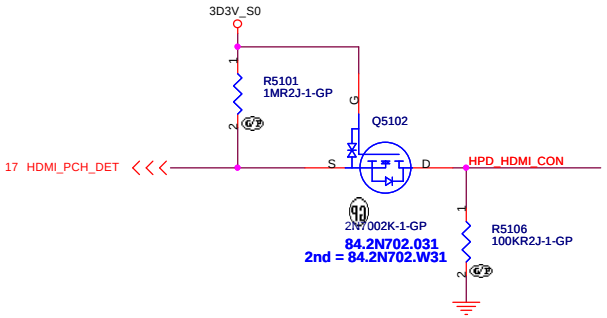


HDMI DDC Passive Level Shifter

R5112,R5111 2.2-kΩ ±5% pull-up to 5 V
after the level shifter for intel check list







JV10-CS

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Title	HDMI Level Shifter/Conn	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 51 of 103	

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Title: *(Reserved)Display Port*

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 52 of 103

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(Blanking)

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Title	*(Reserved)S-Video*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 53 of 103	

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Title	(Reserved)DVI	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 54 of 103	

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Title	(Reserved)ITP	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 55 of 103	

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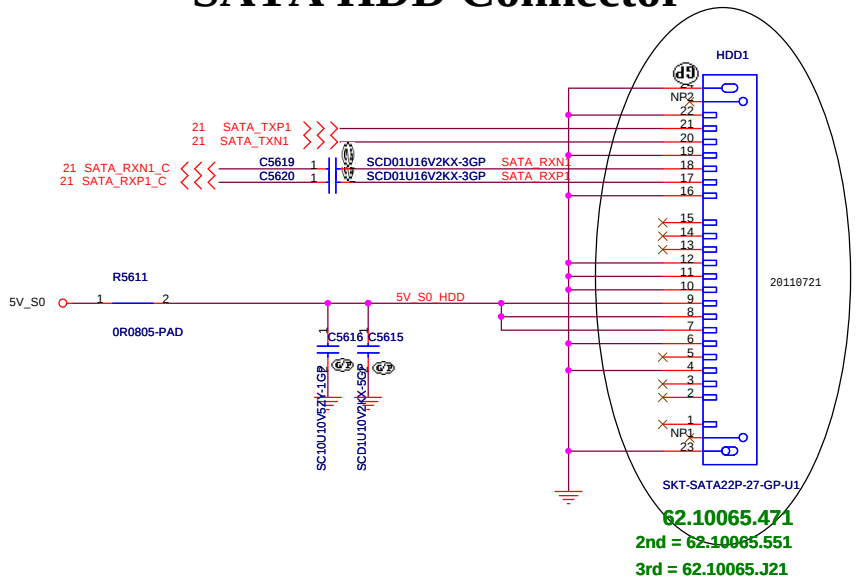
SSID = SATA

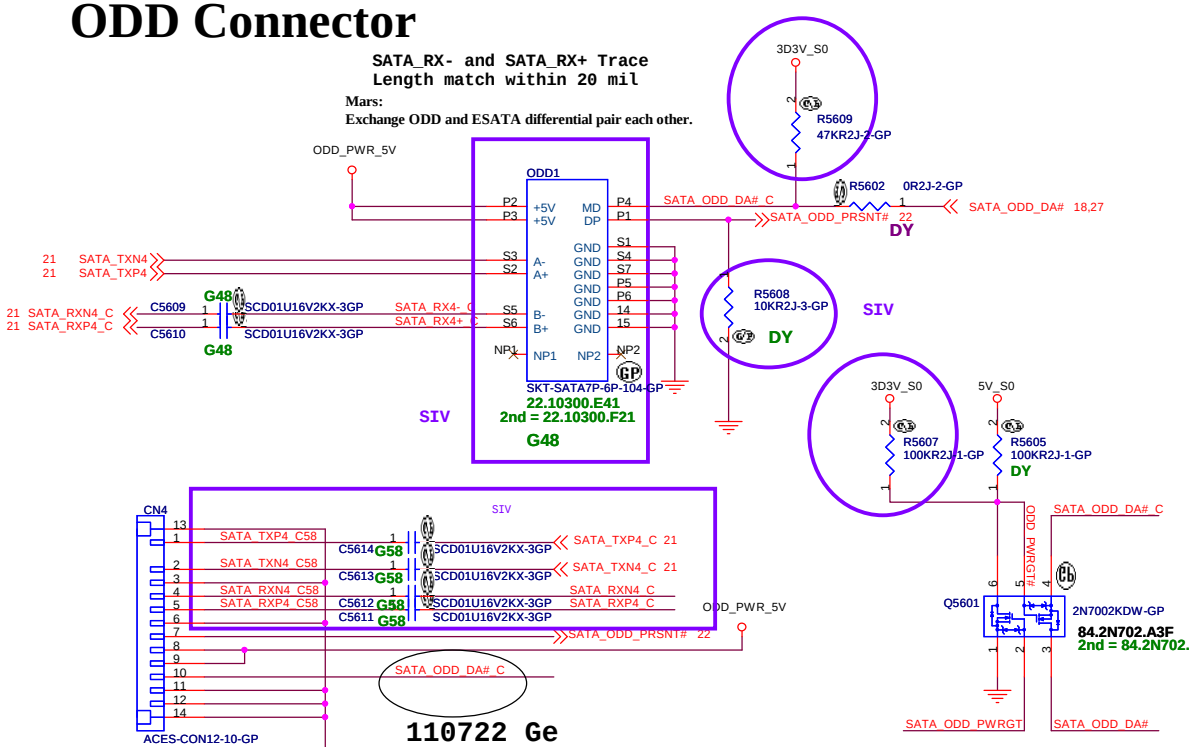
SATA HDD Connector



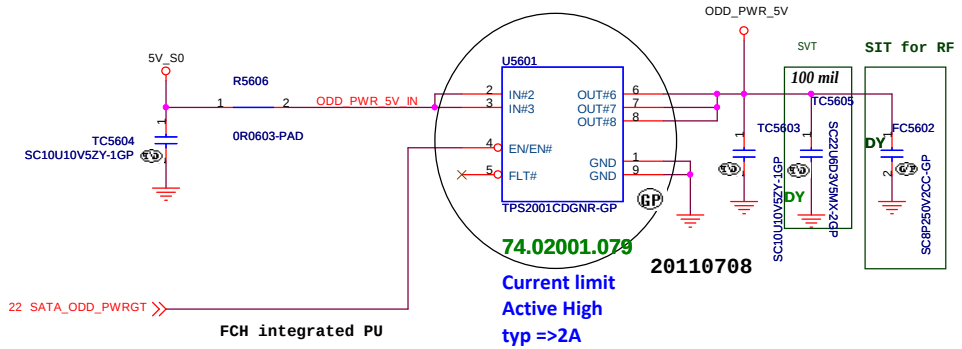
ODD Connector

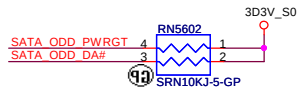
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.



SATA Zero Power ODD





SUPPORT ZERO SATA ODD

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Title: HDD/ODD		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 56 of 103	

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Title	(Reserved)E-SATA	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 57 of 103	

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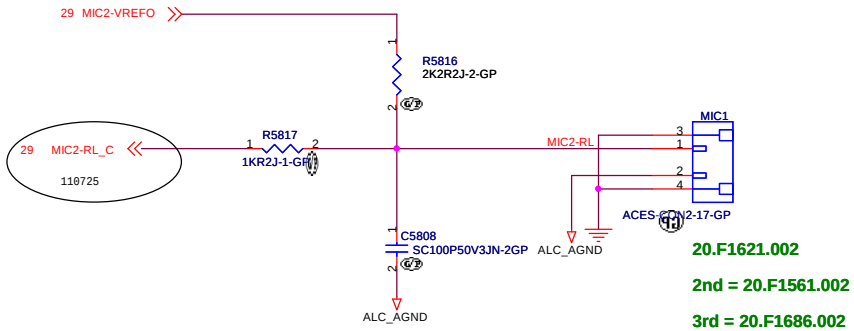
Analog Internal Mic



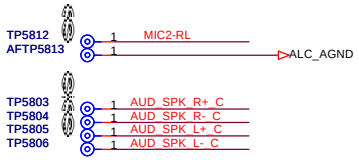
20.F1621.002

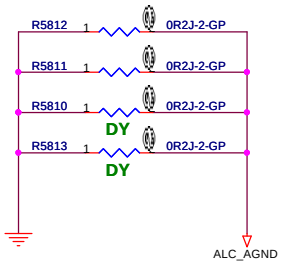
2nd = 20.F1561.002

3rd = 20.F1686.002

4nd = 20.F0693.002

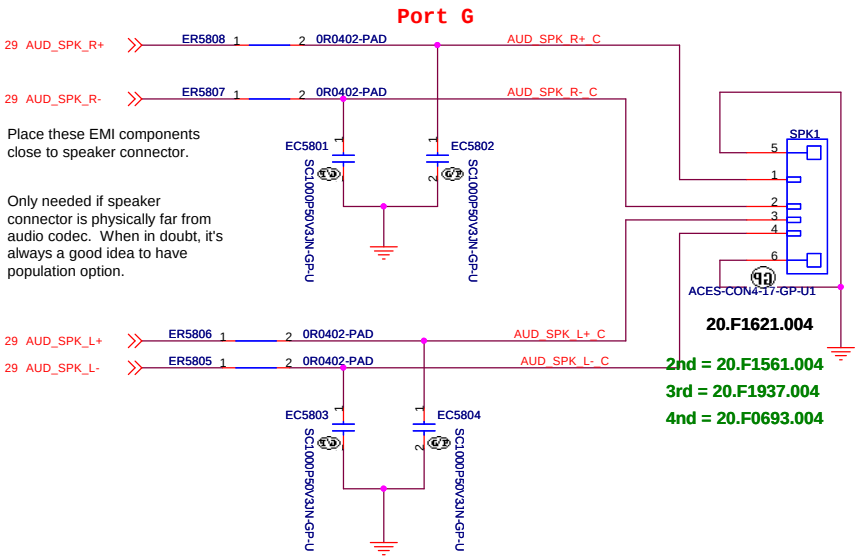
For EMI request:
Change C5801,C5802 to varister 69.80024.001





SIV
Remove bestbuy

INTERNAL STEREO SPEAKERS



20.F1621.004

2nd = 20.F1561.004

3rd = 20.F1937.004

4nd = 20.F0693.004

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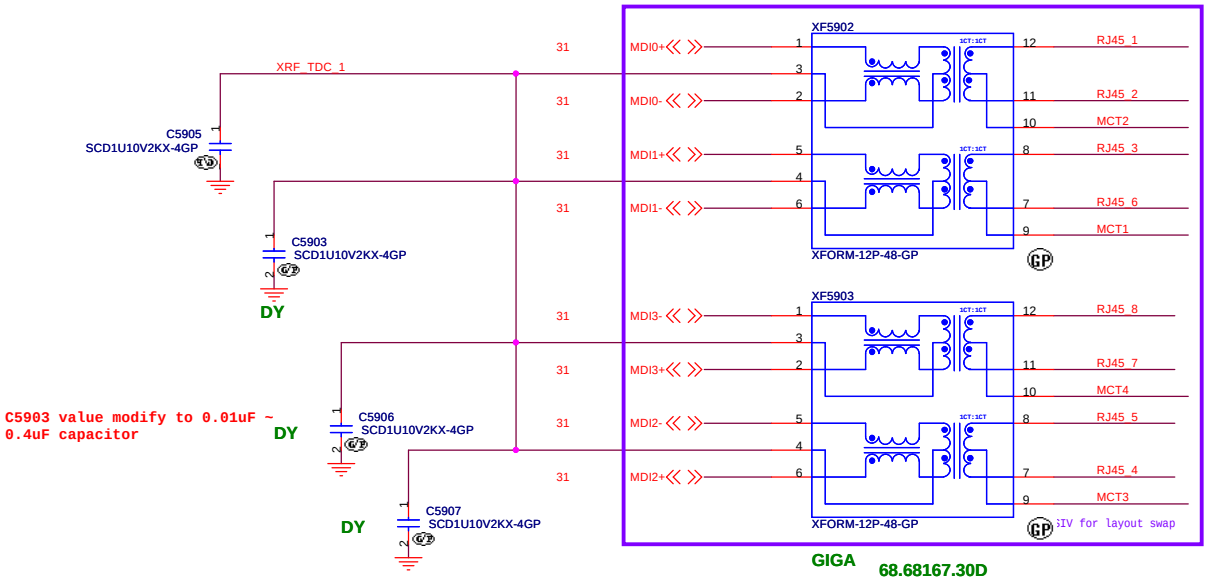
Title	MIC/SPEAKER/AUDIO JACK	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 58 of 103	

10/100M Lan Transformer

FOR CO-LAY GIGA Lan Transformer



68.68167.30D

2nd = 68.0NS14.301

3rd = 68.HD081.30B

68.68167.30D

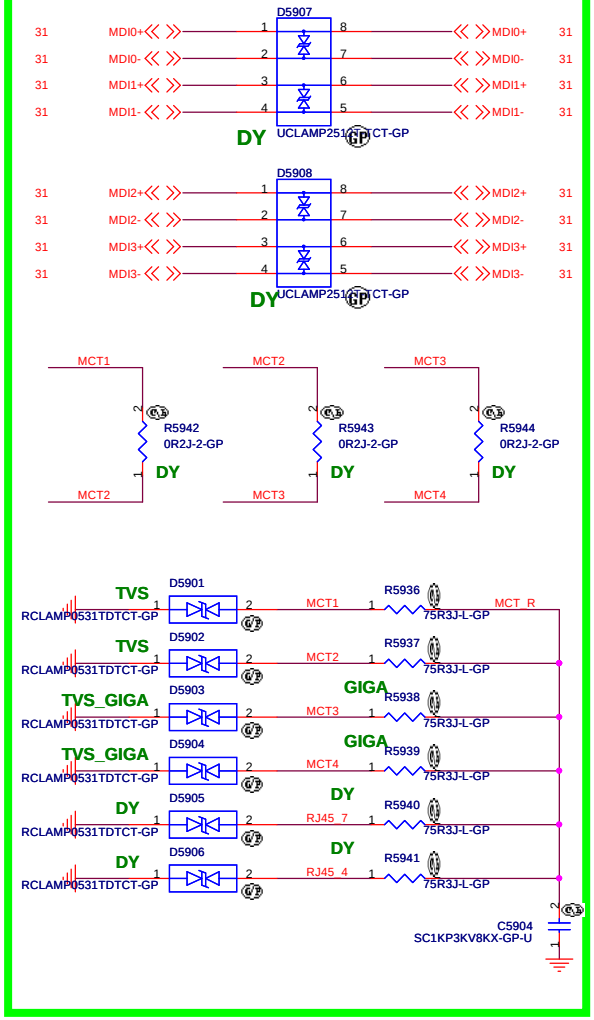
2nd = 68.0NS14.301

3rd = 68.HD081.30B

1.route as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For AR8162(10/100M): C5906, C5907,R5938, R5939 can be DY.
For AR8161(GIGA): Dummy R5934, R5935, R5940,R5941

10/100 LAN surge circuit



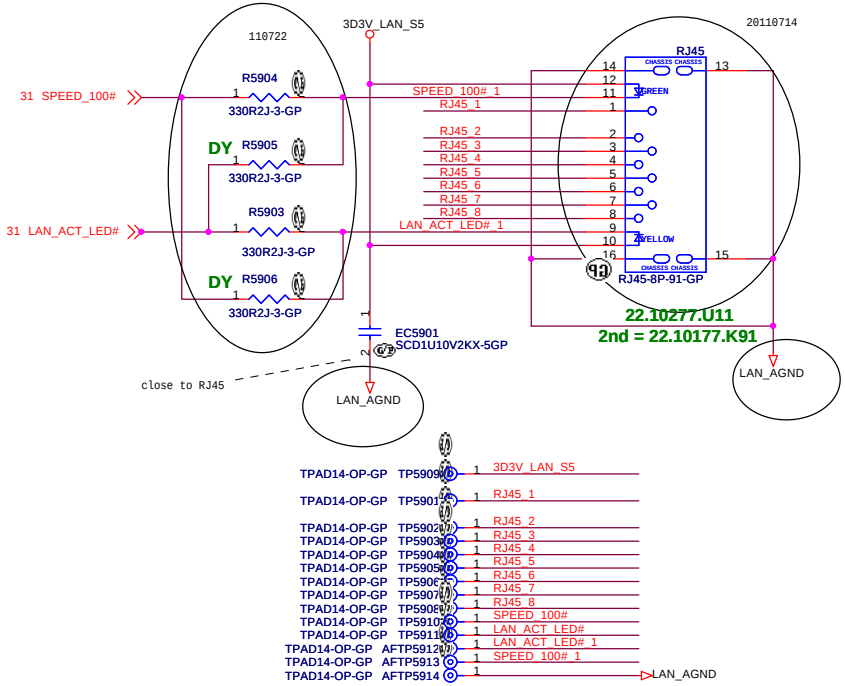
83.00531.0AF
2nd = 83.00511.0A0

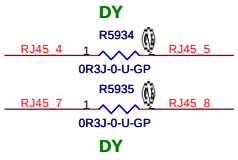
83.00531.0AF
2nd = 83.00511.0A0

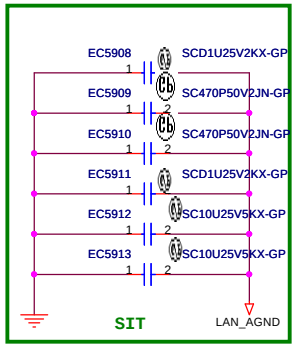
83.00531.0AF
2nd = 83.00511.0A0

83.00531.0AF
2nd = 83.00511.0A0

LAN Connector







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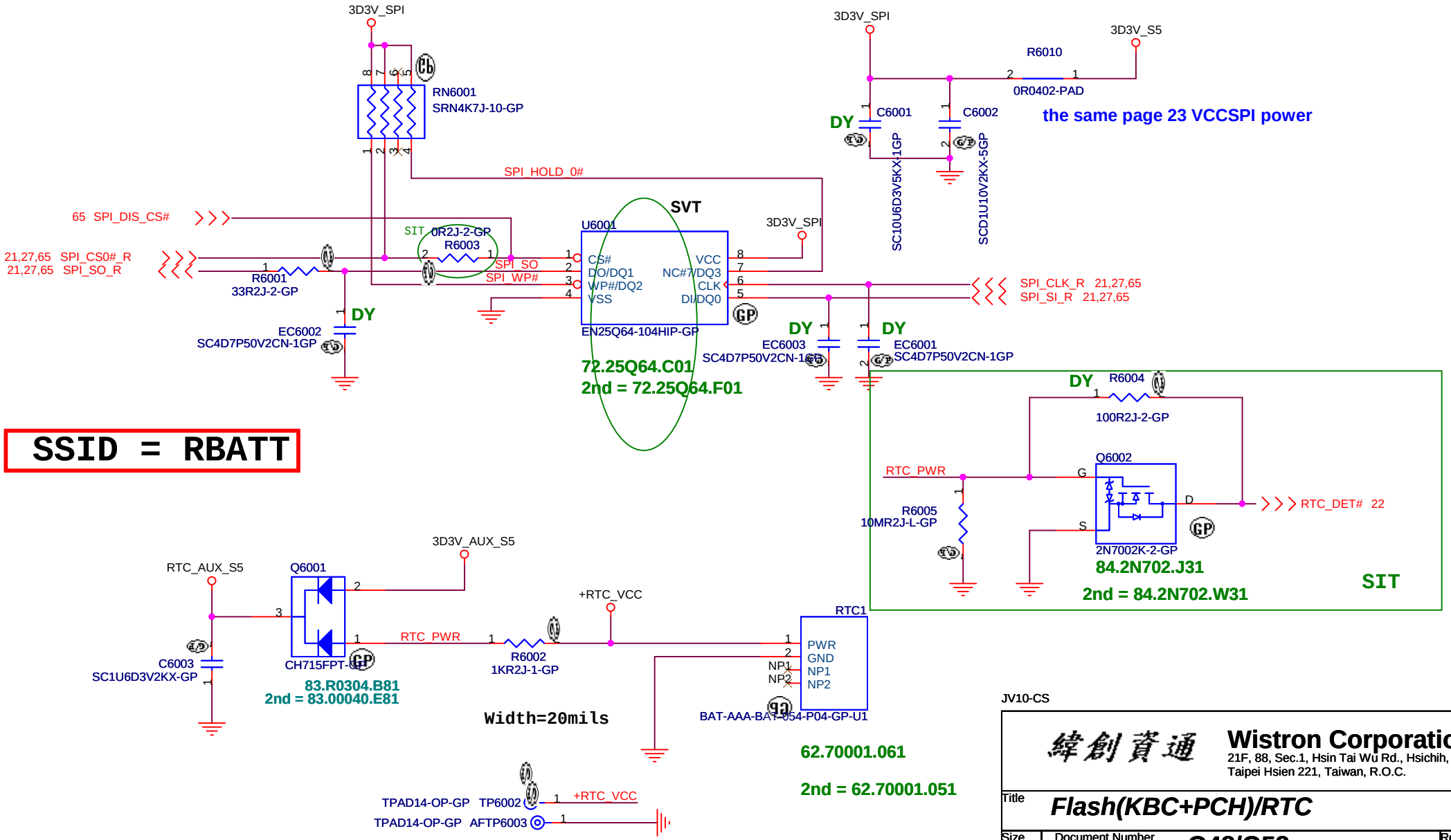
Title	RJ45	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 59 of 103	

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



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Title	Flash(KBC+PCH)/RTC		
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 60 of 103		

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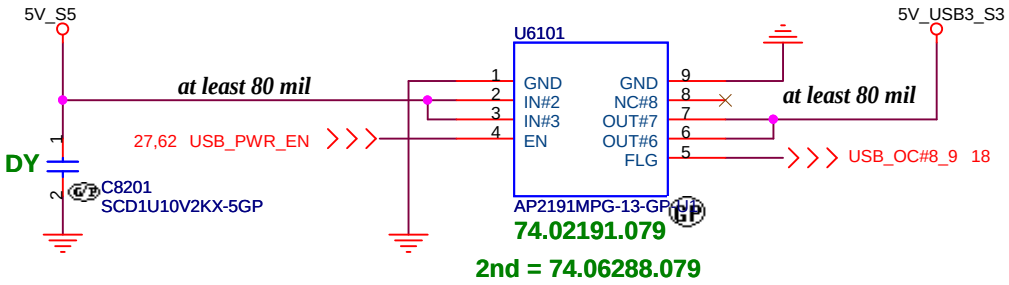
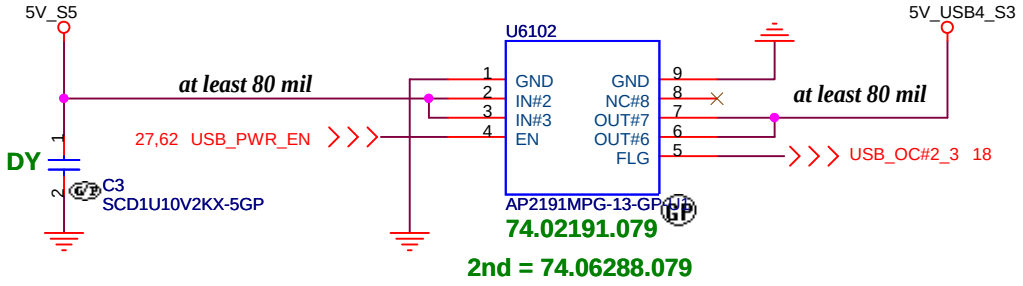
SSID = USB

USB Ext. port3 power SW



U6101 place near to USBCN3

USB Ext. port4 power SW



U6102 place near to CDRCN2

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Title: *USB2.0 Port Power SW*		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 61 of 103	

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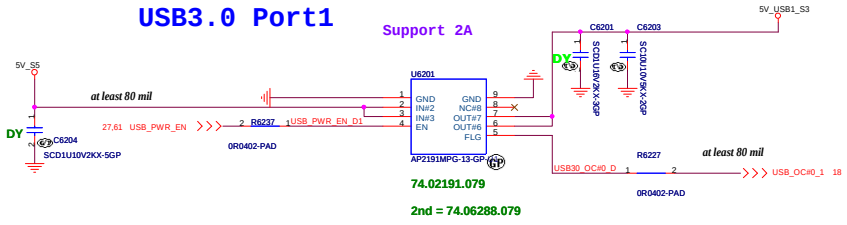
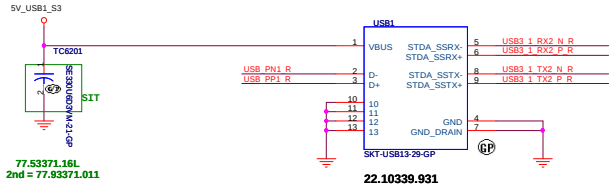
USB3.0 Port1

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

2nd = 77.93371.011

22.10339.931

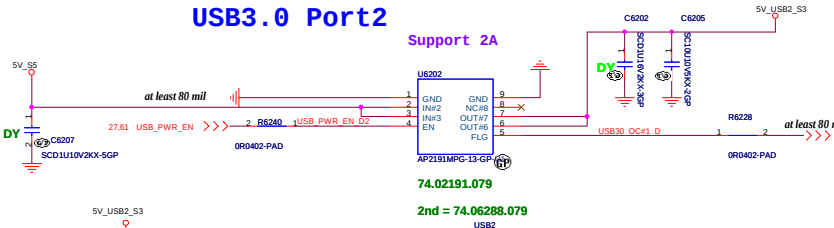
2nd = 22.10339.C11

TC6201 place near
the USB1 connector

Co-Layout USB2.0 22.10321.S01

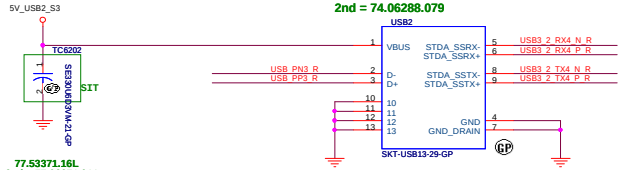
USB3.0 Port2

Support 2A



74.02191.079

2nd = 74.06288.079



77.53371.16L

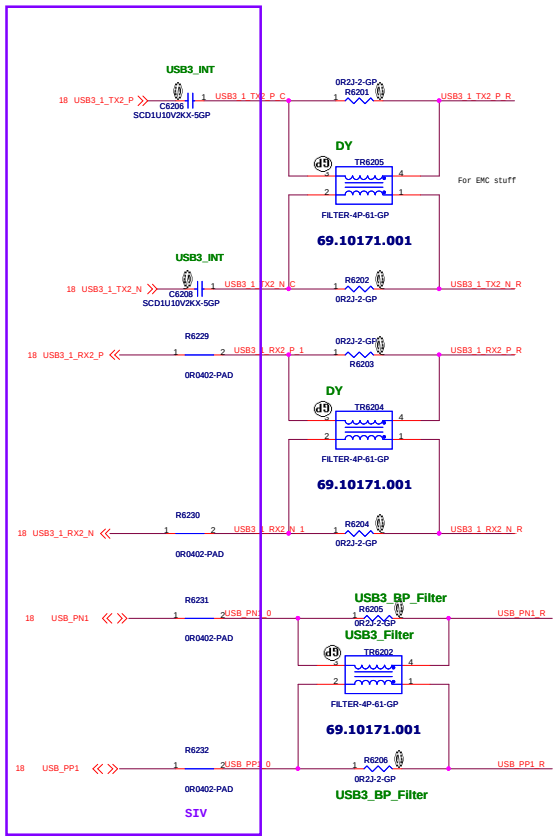
2nd = 77.93371.011

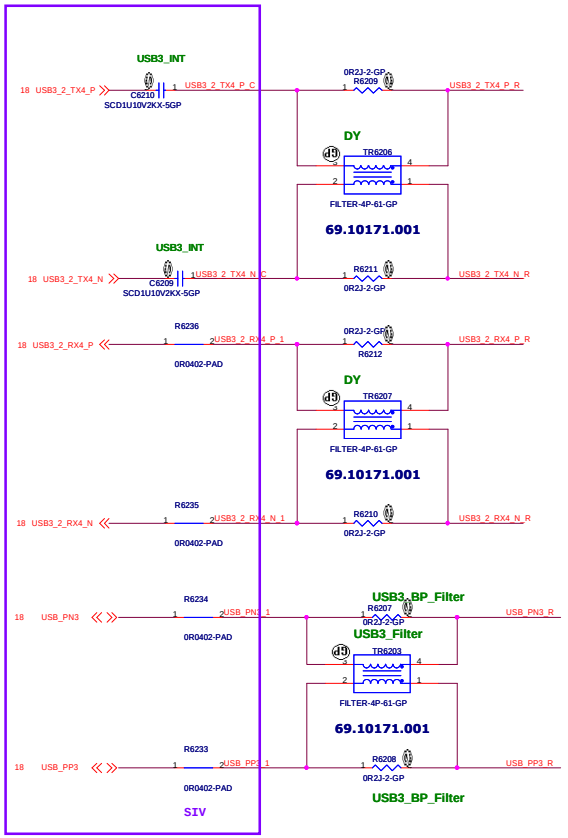
22.10339.931

2nd = 22.10339.C11

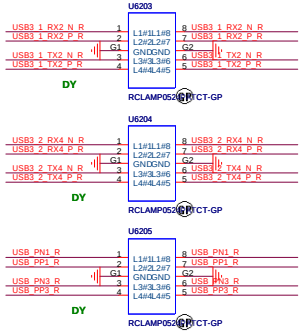
TC6202 place near
the USB2 connector

Co-Layout USB2.0 22.10321.S01





LAN surge circuit



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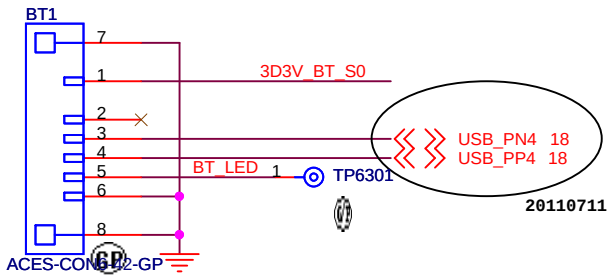
Title: USB3.0 Port1/2

Size: | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 62 of 103

SSID = User.Interface

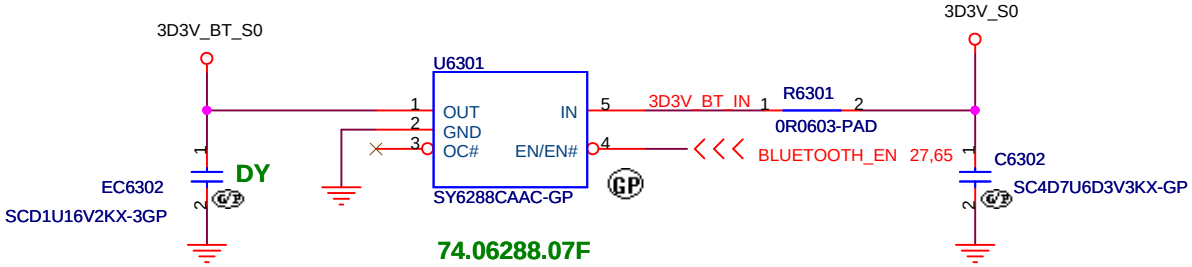
Bluetooth conn.



20.F1705.006

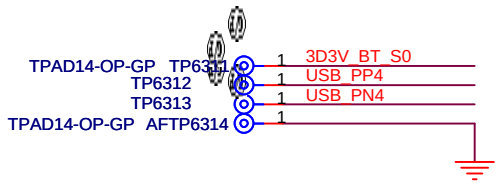
2nd = 20.F1804.006

3rd = 20.F1571.006



74.06288.07F

EC6302 put near BLUE1 / all USB put one choke near connector by EMI request



JV10-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BLUETOOTH***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 63 of 103	

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***(Reserved)Finger Print Con.***	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 64 of 103	

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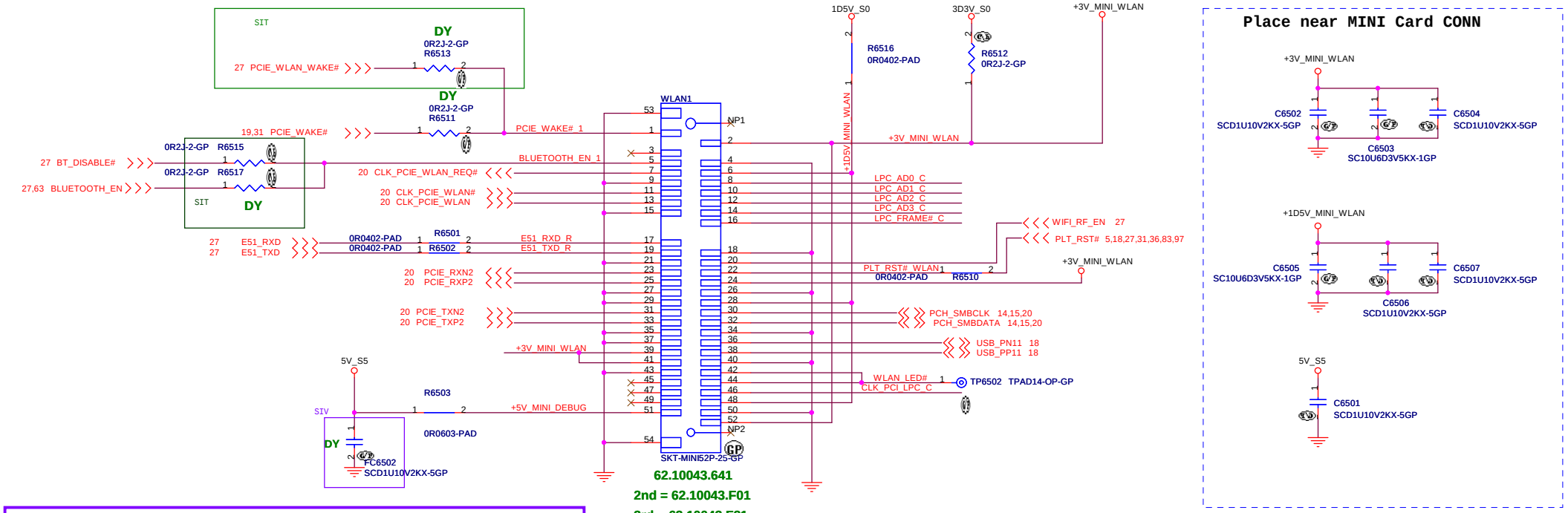
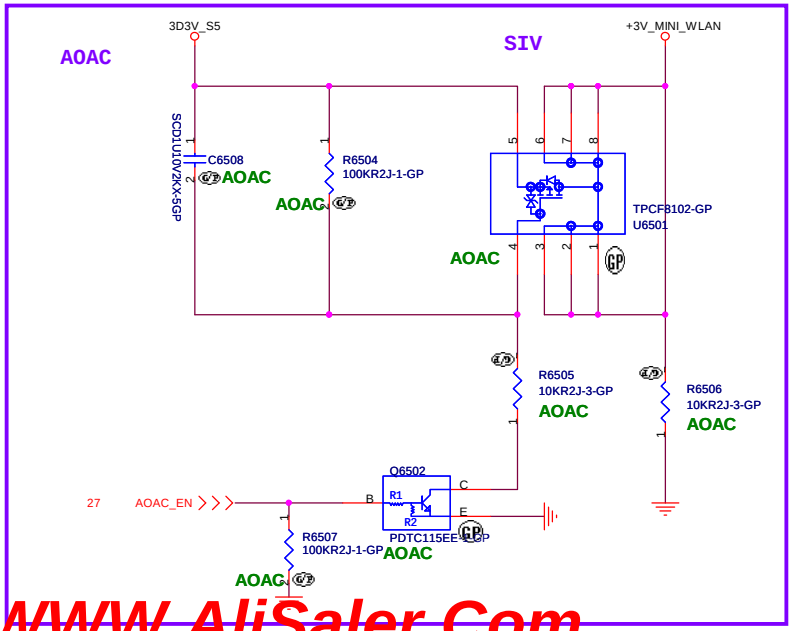
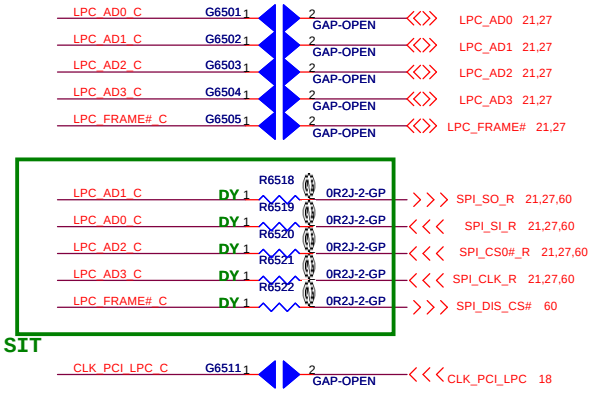
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)







JV10-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: WLAN		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 65 of 103	

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SSID = Wireless

Mini Card Connector(WWAN)

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)WWAN CONN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 66 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)3rd MINICARD	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 67 of 103	

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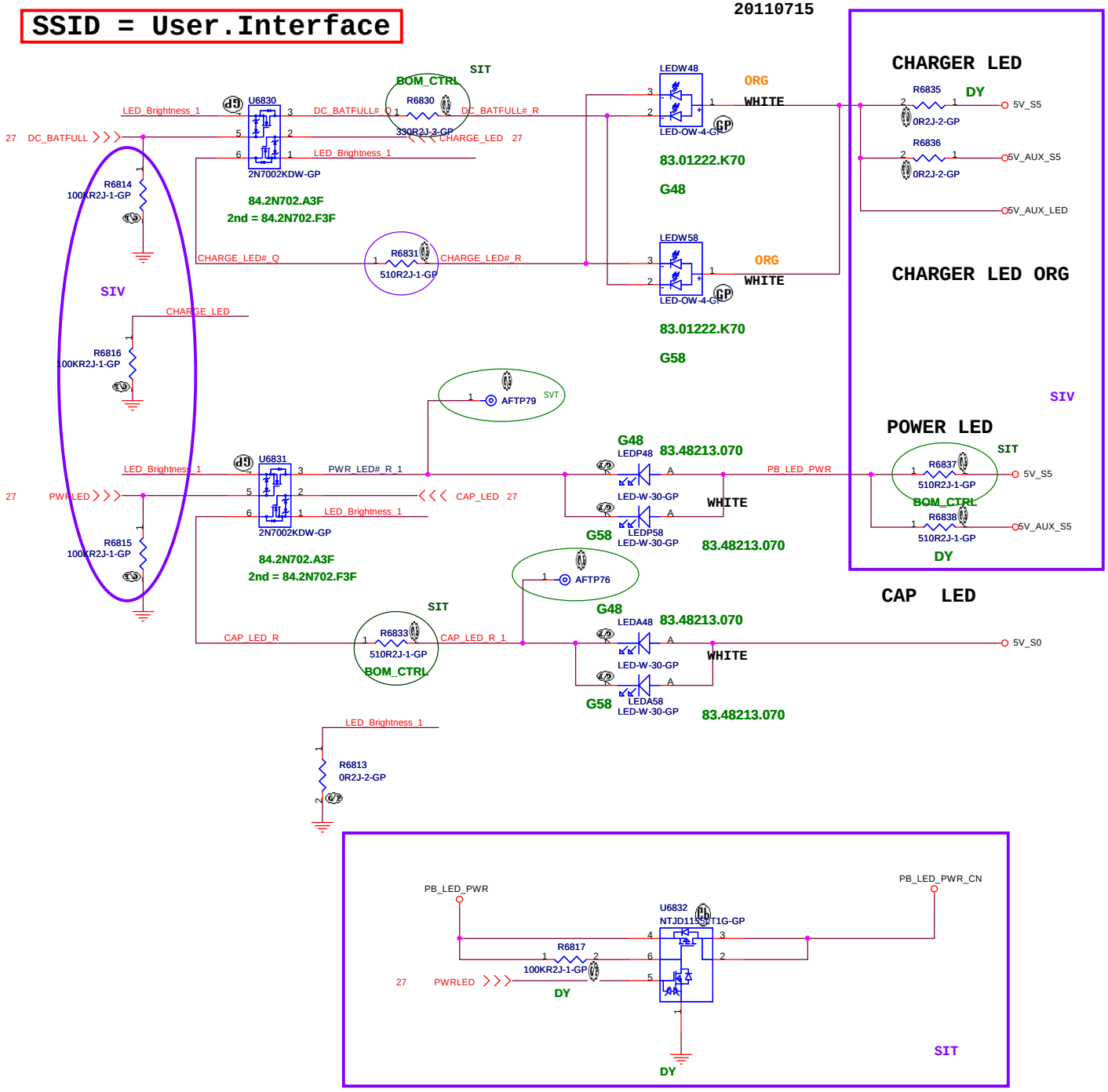
20110715

SSID = User.Interface



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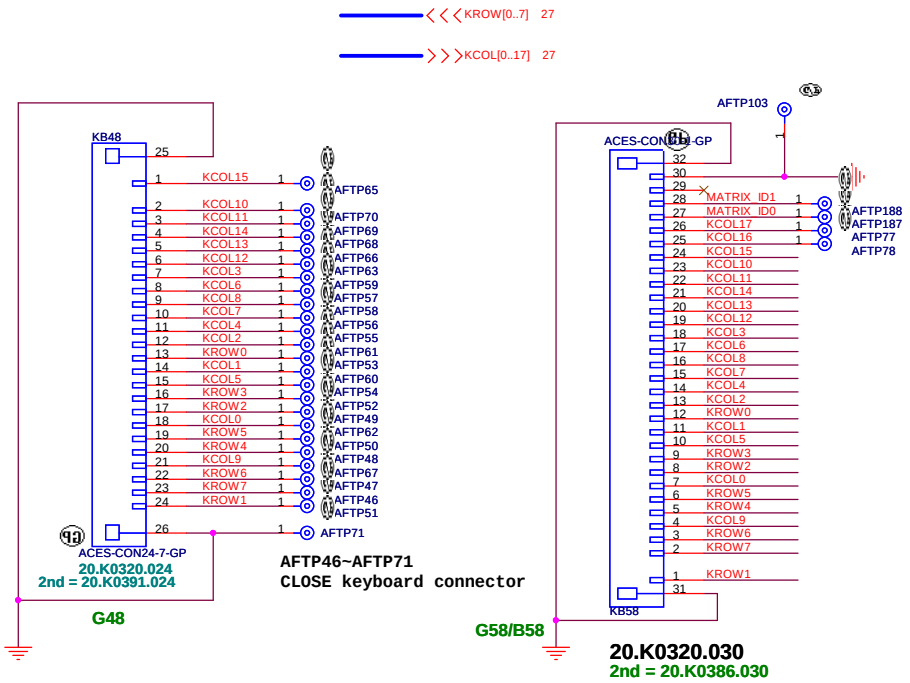
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LED/Power Button/key
Size	Document Number: G48/G58 — Rev: SC
Date: Friday, February 17, 2012	Sheet 68 of 103

SSID = KBC

KB1 Follow LA47

Internal KeyBoard Connector



14"

* Membrane Pin Out Top View :

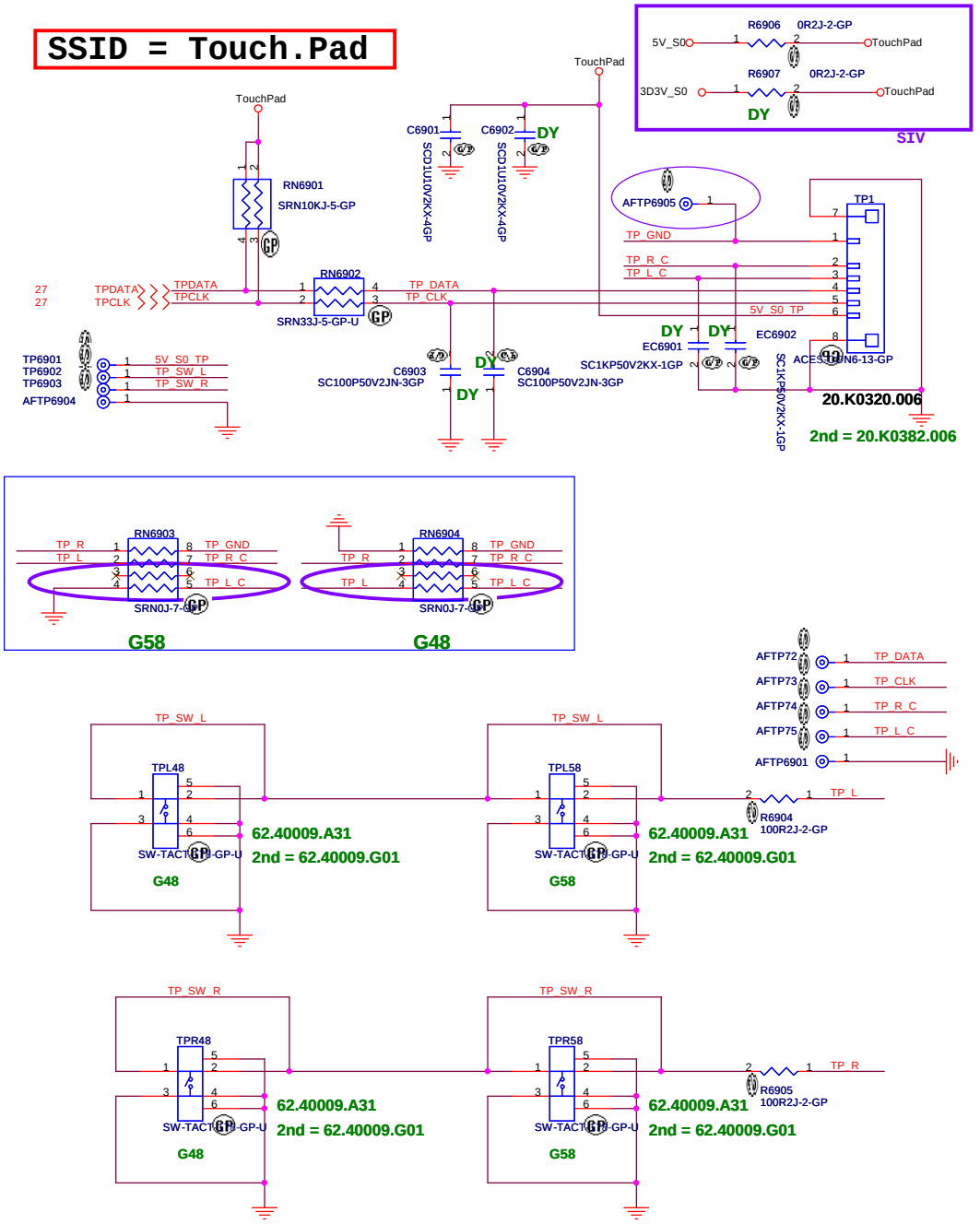
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

15"

* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	25	26	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	D 17	D 18	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



JV10-CS

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Key Board/Touch Pad	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 69 of 103	

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緯創資通 **Wistron Corporation**
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Title ***Hall Sensor***

Size	Document Number	Rev
	G48/G58	**SC**

Date: Friday, February 17, 2012 Sheet 70 of 103

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *(Reserved)Debug connector*

Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 71 of 103

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Title	(Reserved)RJ11+MDC	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 72 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)1394 CONN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 73 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)CARD Reader CONN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 74 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Express Card	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 75 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Smart Card Socket	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 76 of 103	

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Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)TPM	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 77 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)SIO	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 78 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)G-Sensor	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 79 of 103	

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Title	(Reserved)RF/Other	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 80 of 103	

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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)Screw Holes,SPR	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 81 of 103	

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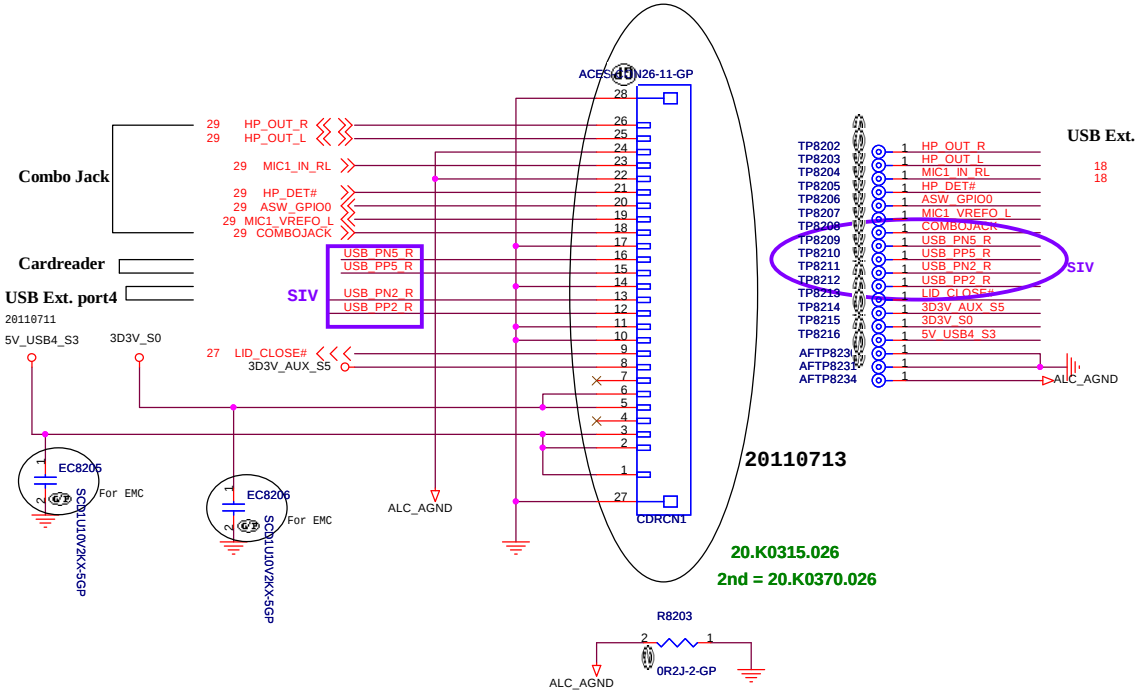
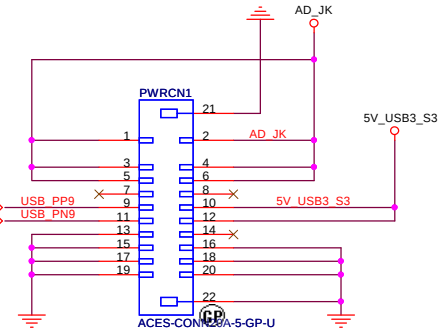
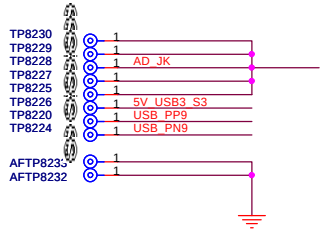
Cardreader BD connector
(Cardreader/Combo Jack/USB2.0 port4)

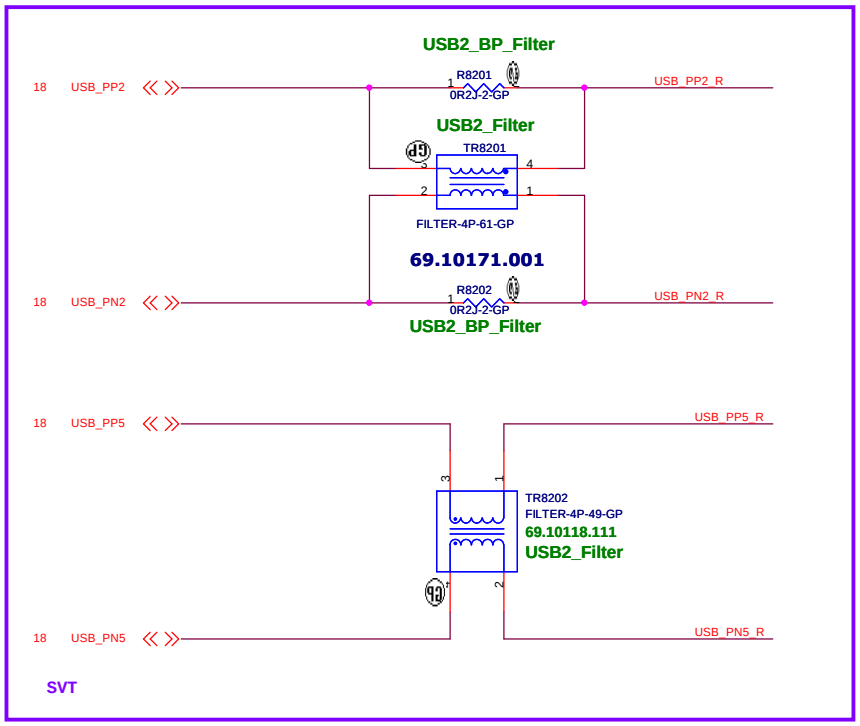


USB Ext. port3

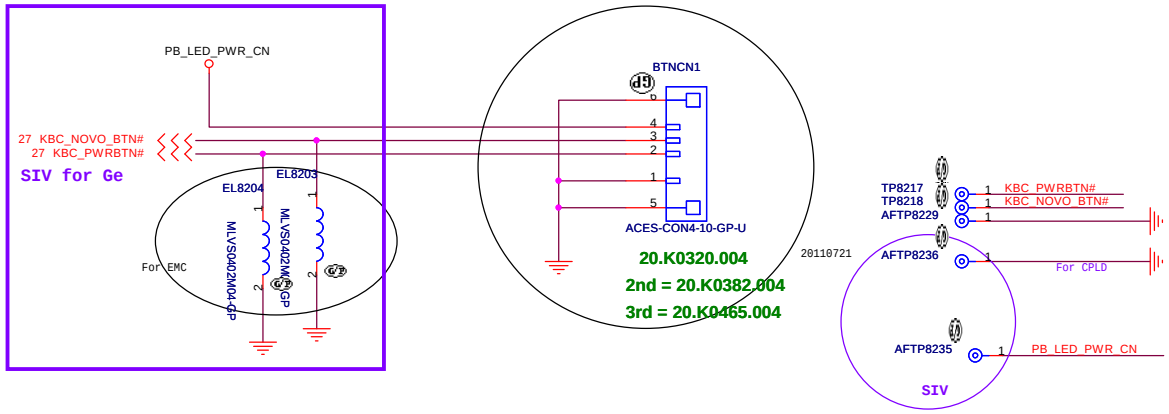
USB BD connector
(DC Jack/USB2.0 port3)







Button BD connector
(Power button/NOVO button)



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: IO Board Connector		
Size	Document Number: G48/G58	Rev: SC
Date: Friday, February 17, 2012	Sheet 82 of 103	

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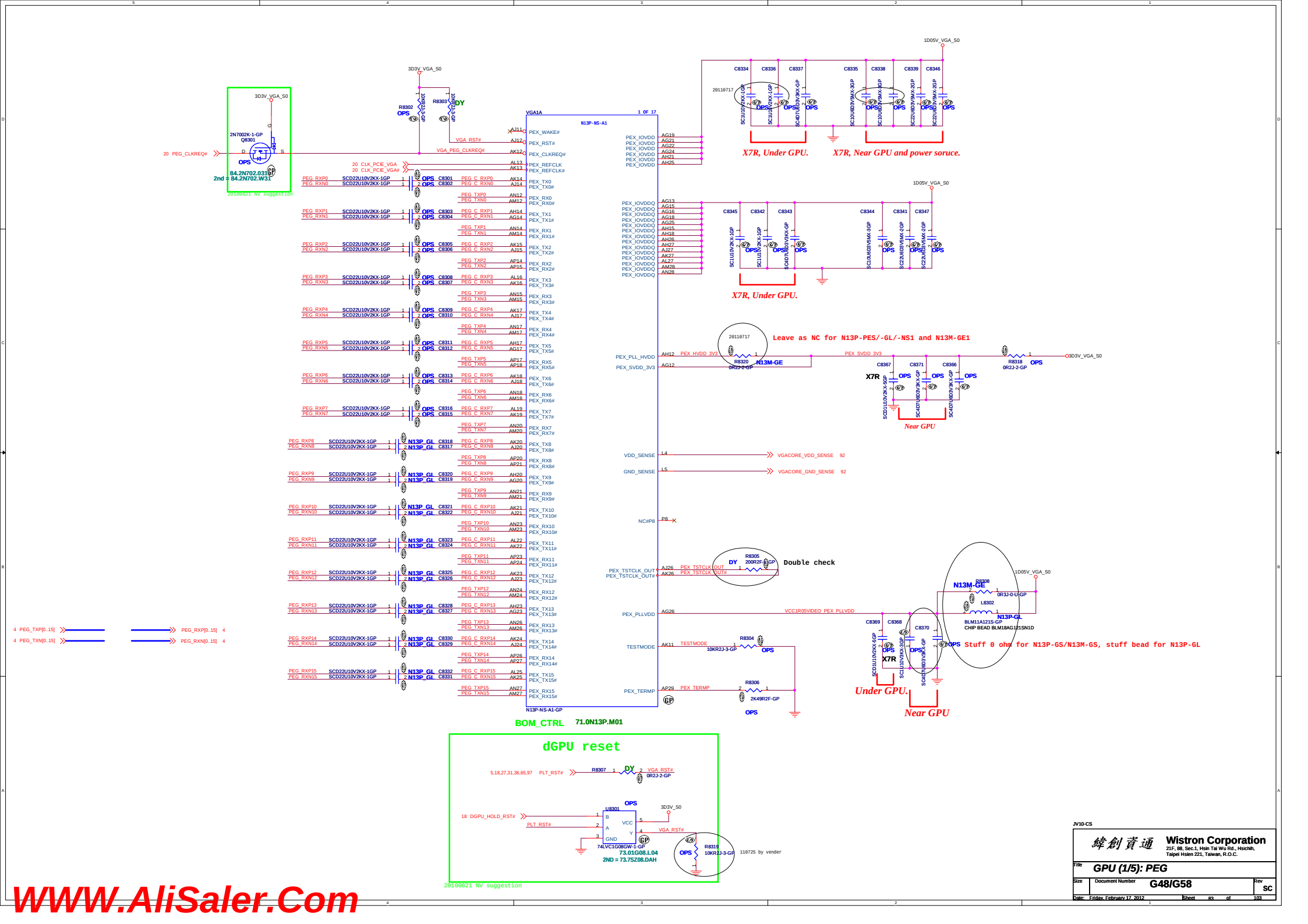
VGA1A
1 OF 17
N13P-NS-A1
N13P-NS-A1-GP
PEX_WAKE#
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
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PEX_TX15
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PEX_RX15
PEX_RX15#
PEX_IOVDD
PEX_IOVDDQ
PEX_PLL_HVDD
PEX_SVDD_3V3
VDD_SENSE
GND_SENSE
NC#P8
PEX_TSCLK_OUT
PEX_TSCLK_OUT#
PEX_PLLVDD
TESTMODE
PEX_TERMP
VGACORE_VDD_SENSE 92
VGACORE_GND_SENSE 92
X7R, Under GPU.
X7R, Near GPU and power soruce.
X7R, Under GPU.
Leave as NC for N13P-PES/-GL/-NS1 and N13M-GE1
Near GPU
Double check
Under GPU.
Near GPU
Stuff 0 ohm for N13P-GS/N13M-GS, stuff bead for N13P-GL
BOM_CTRL 71.0N13P.M01
dGPU reset
20110621 NV suggestion
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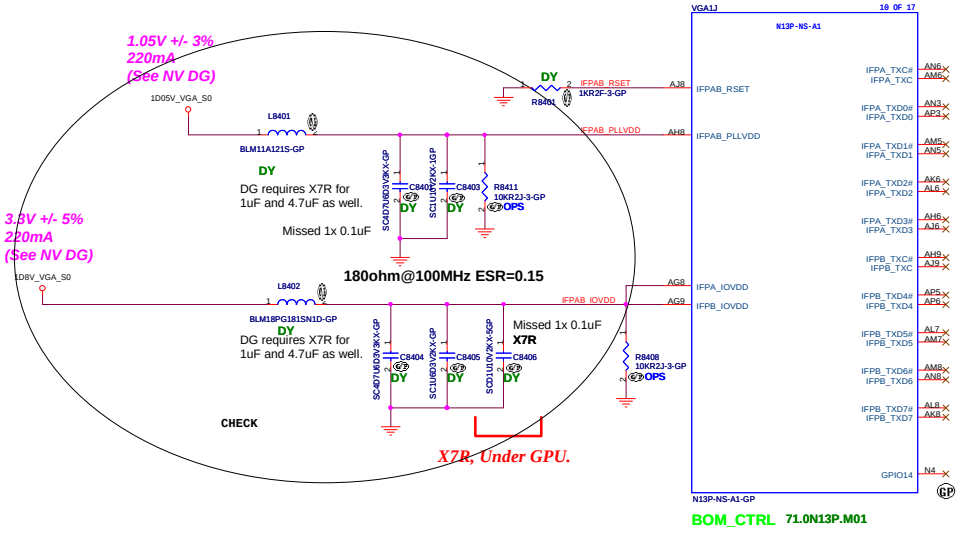
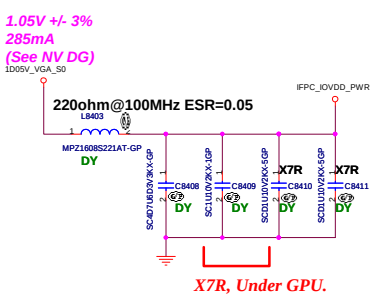
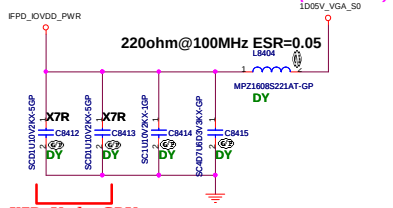
Wistron Corporation
GPU (1/5): PEG
G48/G58
Friday, February 17, 2012

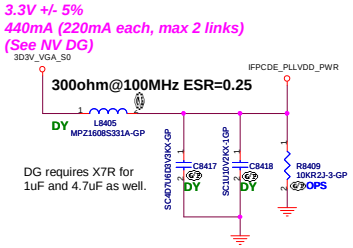
RD480_SA:71.0N12P.M08

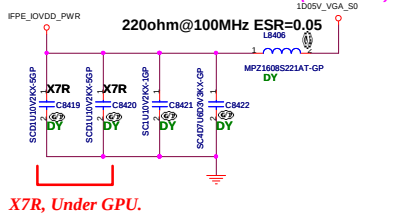
LVDS Interface

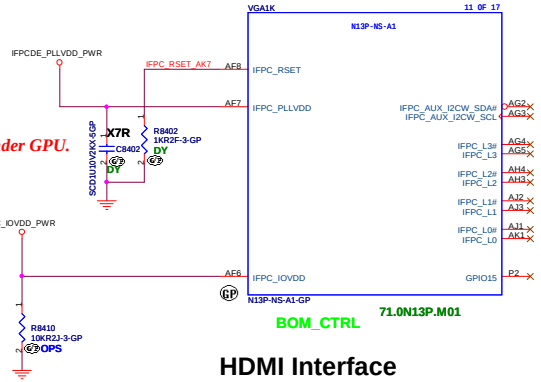




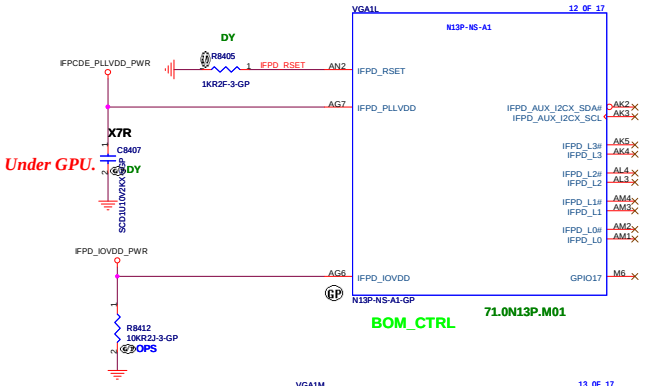


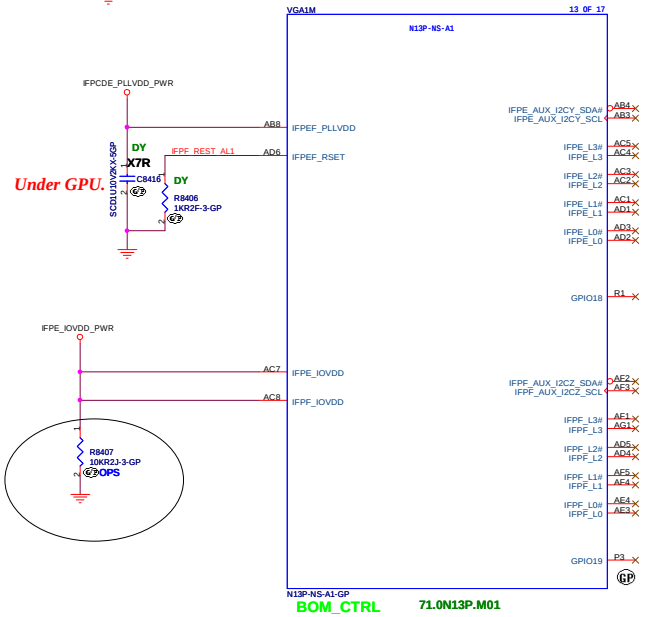






HDMI Interface





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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (2/5): DIGITALOUT

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 84 of 103

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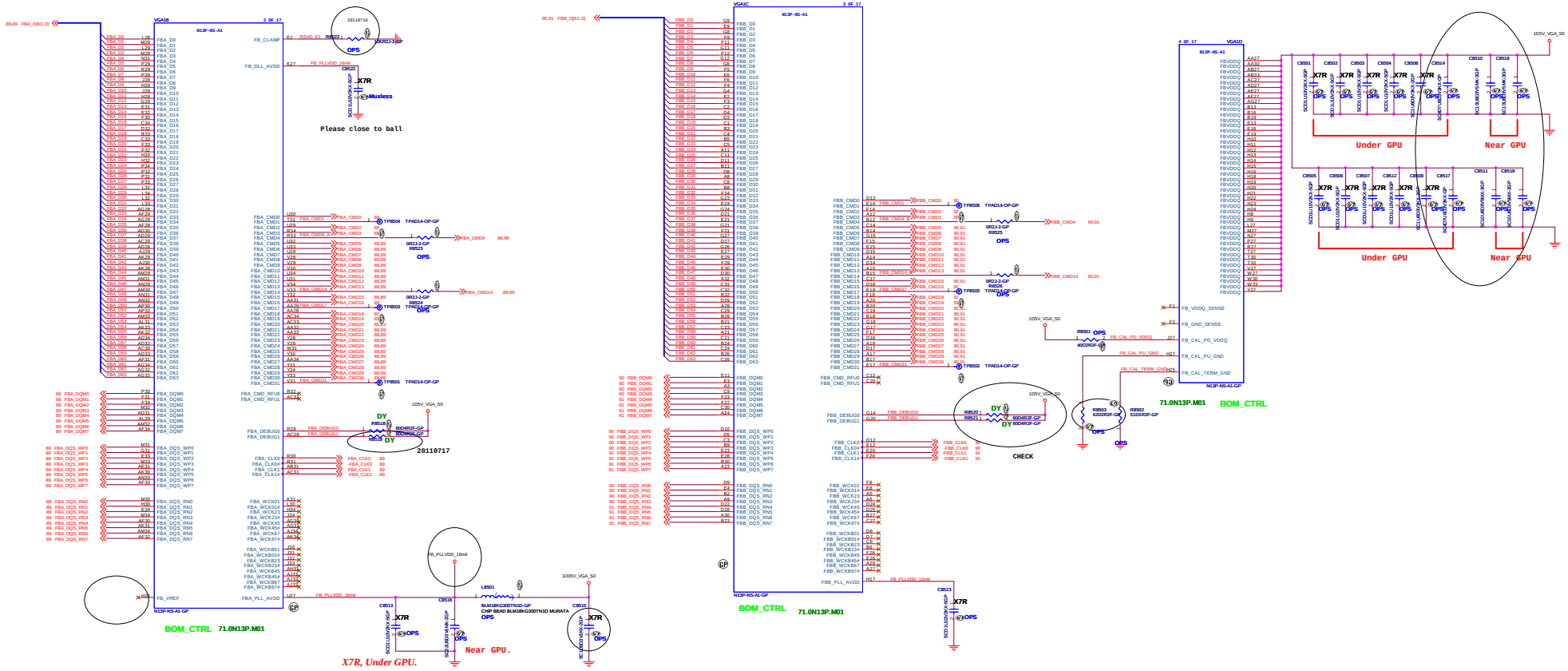
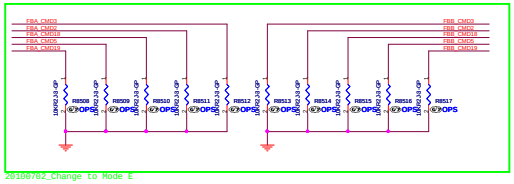


FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

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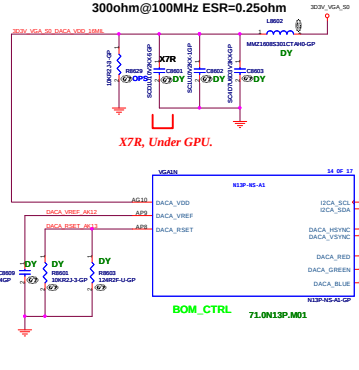
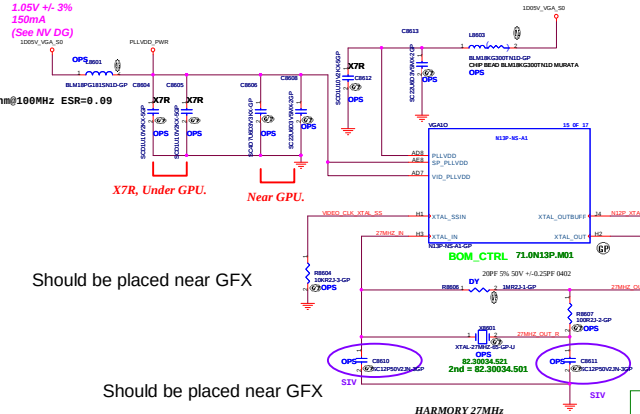
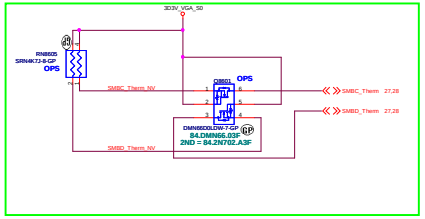
JV10-CS			
Wistron Corporation			
Title	GPU (3/5): VRAM I/F		
Size	Document Number	G48/G58	Rev SC
Date: Friday, February 17, 2012		Sheet 85 of 103	

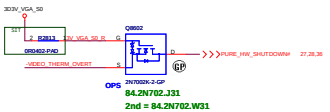
RD480_SA:71.0N12P.M08

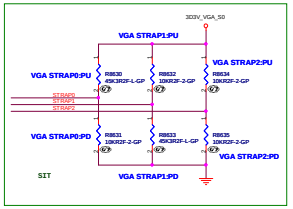


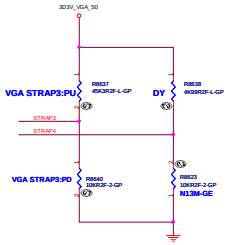


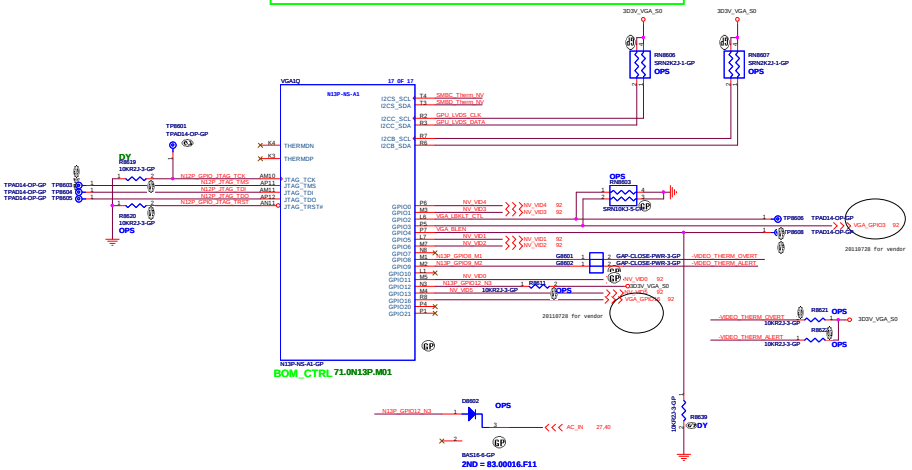


I2CA=>CRT, I2CC=>LVDS.









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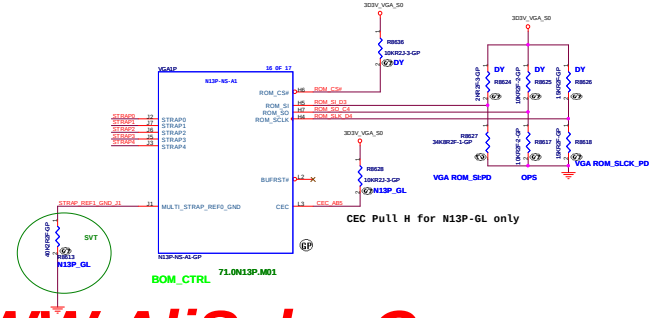
STRAP0	R8630(PU)	45.3Kohm 64.45325.6DL
	R8631(PD)	DY
STRAP1	R8632(PU)	DY
	R8633(PD)	45.3Kohm 64.45325.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL
	R8635(PD)	DY
STRAP3	R8637(PU)	DY
	R8640(PD)	DY
STRAP4	R8638(PU)	DY
	R8623(PD)	DY

	N13M-GE(PS)				
	TABLE NVIDIA	SAMSUNG 128Mx16 72.42164.D0U	SAMSUNG 128Mx16 72.42164.G0U	HYNIX 128Mx16 72.52G63.C0U	Samsung 64Mx16	HYNIX 64Mx16
STRAP0	R8630(PU)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8631(PD)	DY	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP1	R8632(PU)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
	R8633(PD)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
STRAP2	R8634(PU)	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL
	R8635(PD)	DY	10Kohm 64.10025.6DL	DY	10Kohm 64.10025.6DL	DY
STRAP3	R8637(PU)	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	DY	DY
	R8640(PD)	10Kohm 64.10025.6DL	DY	DY	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
STRAP4	R8638(PU)	DY	DY	DY	DY	DY
	R8623(PD)	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL



VGA	N13P-GL(PS) 71.0N13P.E0U	N13M-GE(PS) 71.0N13M.B1U
ROM_SO PD R8617	10Kohm 64.10025.6DL	10Kohm 64.10025.6DL
ROM_SCLK PD R8618	15Kohm 64.15025.6DL	10Kohm 64.10025.6DL

TABLE
VIDEO MEMORY

Nvidia VGA	900MHz	HYNIX 128Mx16	SAMSUNG 128Mx16	HYNIX 64Mx16	Samsung 64Mx16
		72.52G63.C0U	72.42164.D0U 72.42164.G0U	72.51G63.H0U	72.41646.Q0U
N13P-GL	ROM_SI PD R8627	30.1Kohm 64.30125.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL
N13M-GE	ROM_SI PD R8627	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL	10K ohm 64.10025.6DL

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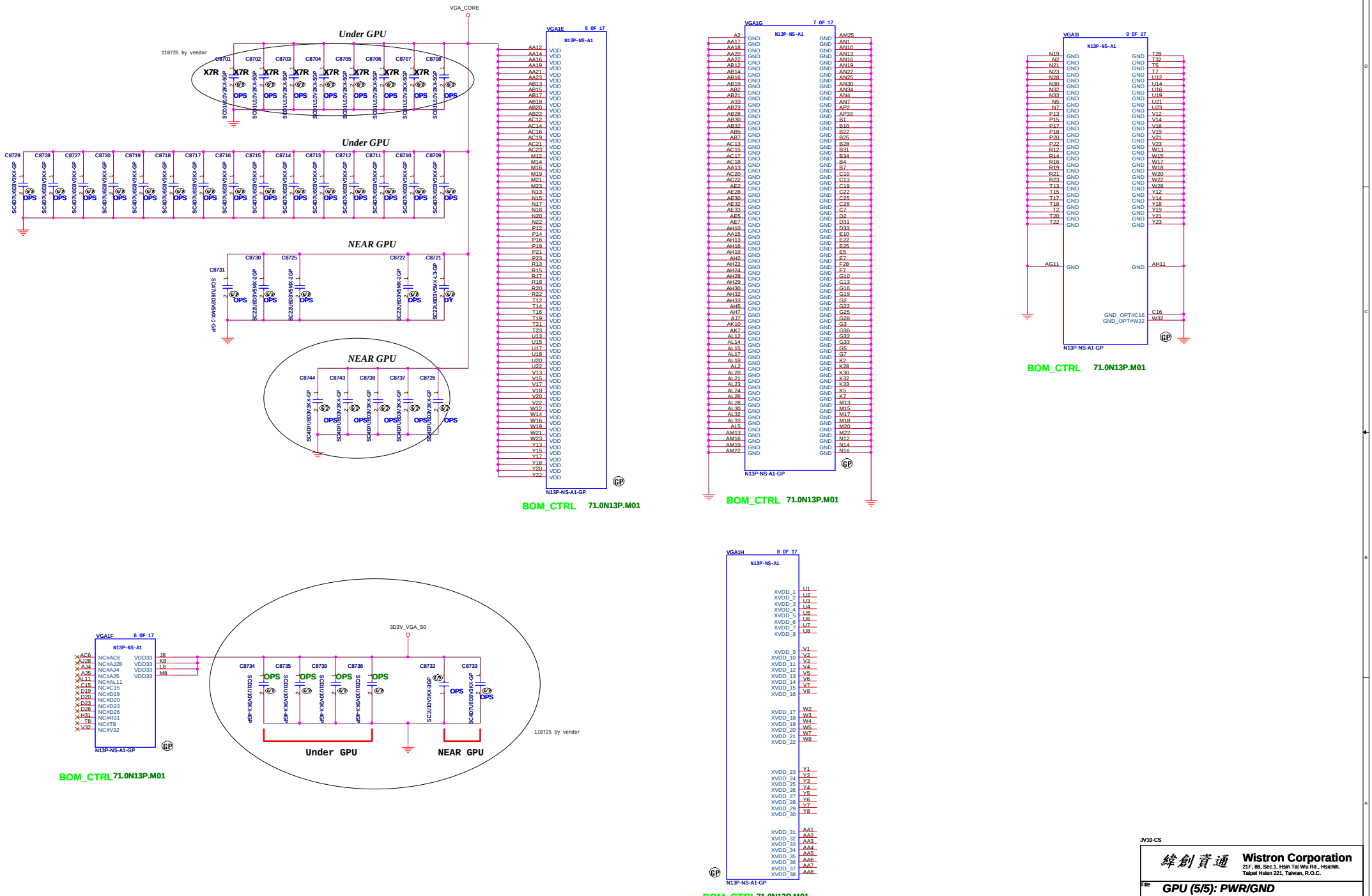
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (4/5): GPIO/STRAP
Size: G48/G58
Document Number
Rev: SC
Date: Friday, February 17, 2012
Sheet 85 of 103



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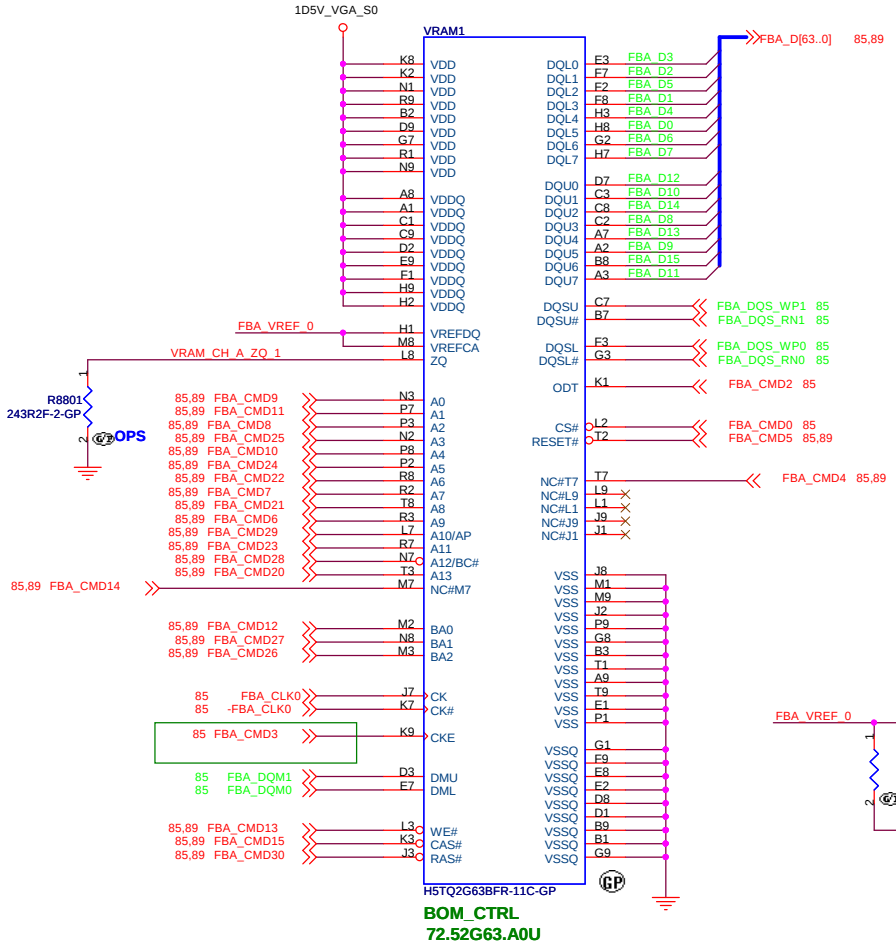
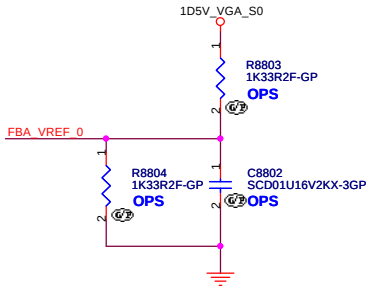
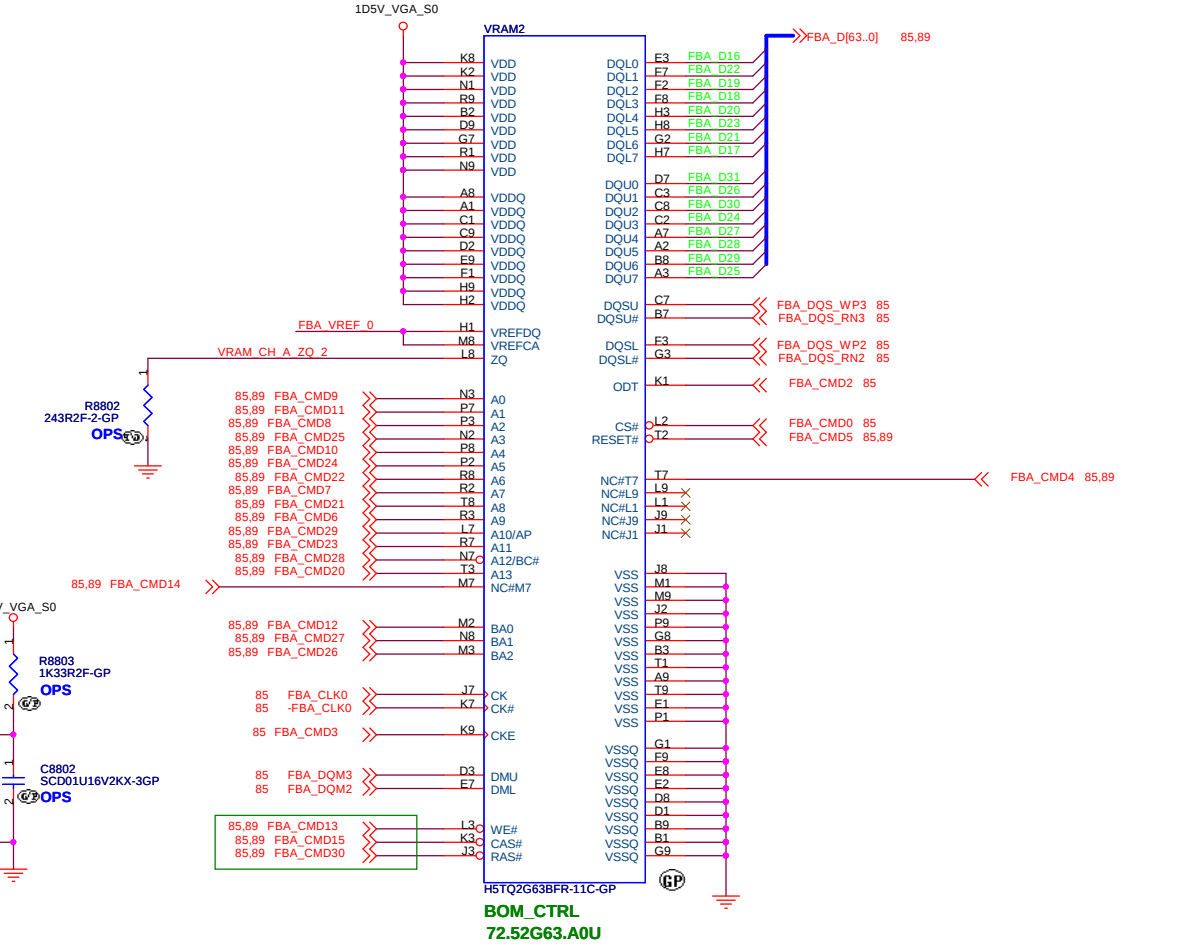
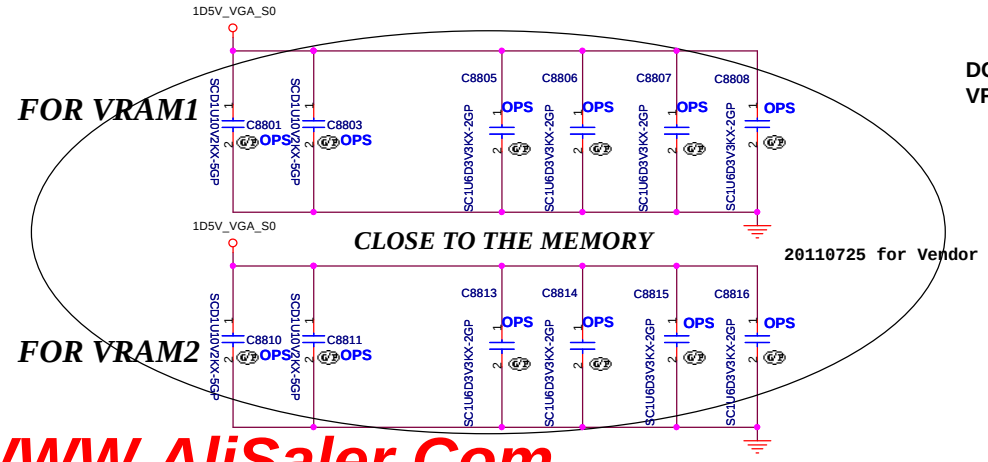


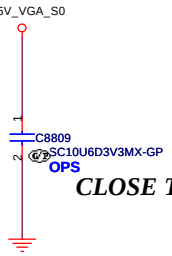






20110725 for Vendor

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VRAM

SAMSUNG:

K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz

K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:

H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz

H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT A

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM1,2 (1/4)		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 88 of 103		

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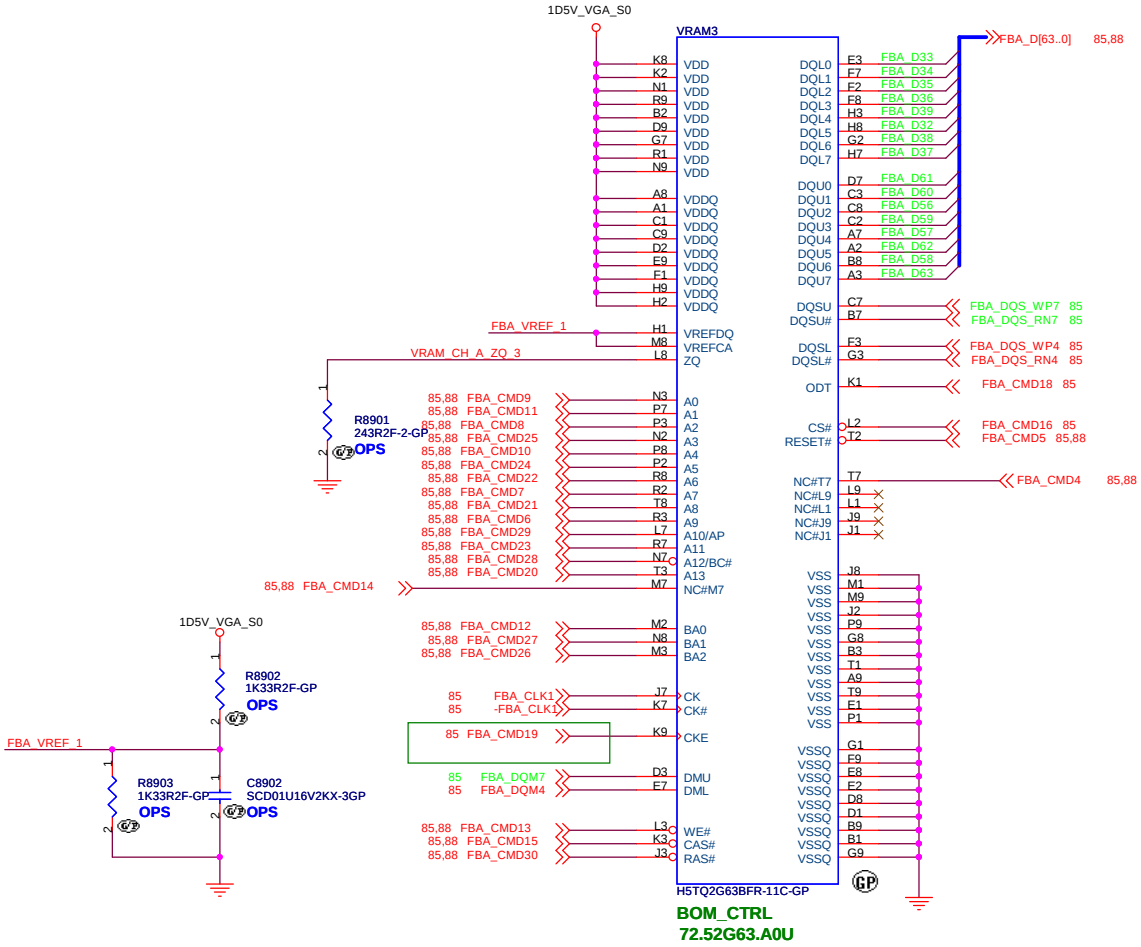

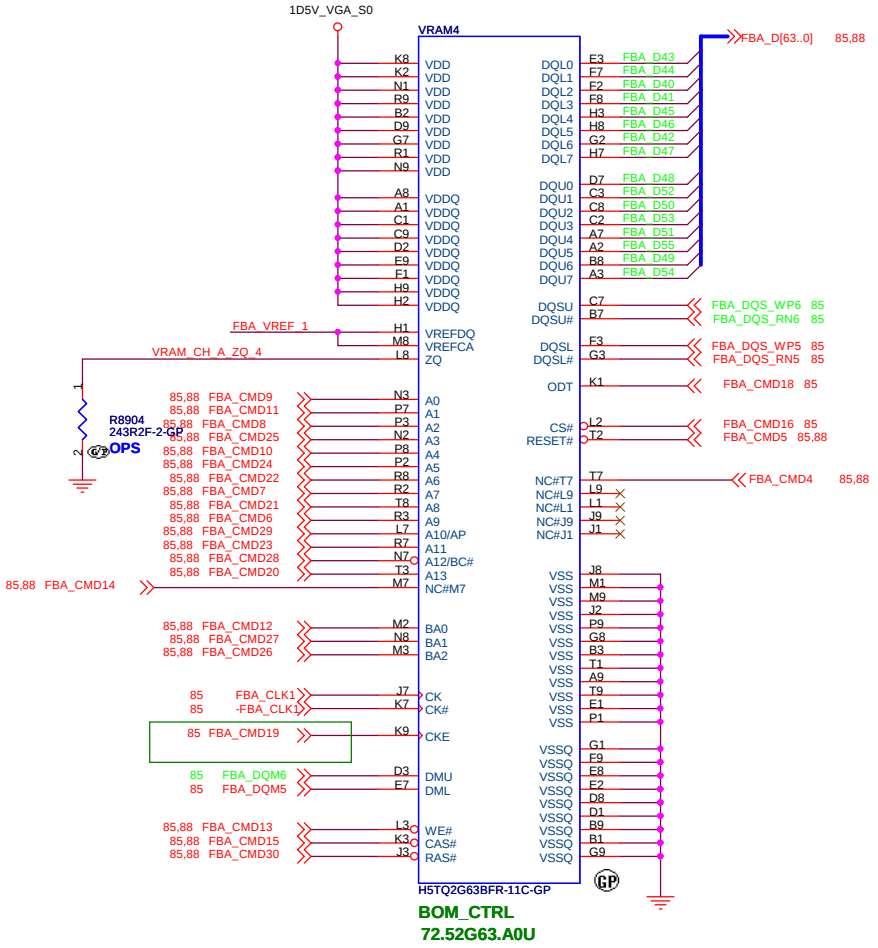

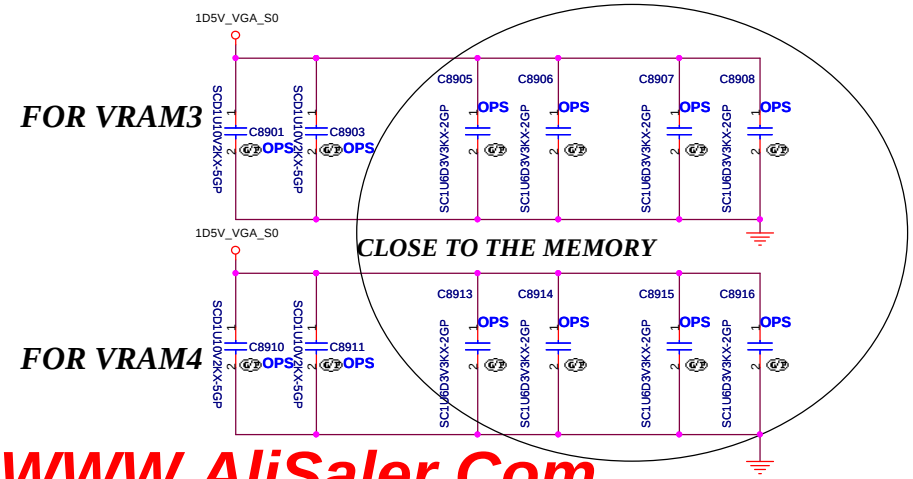

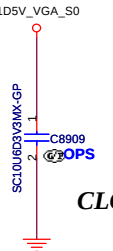

CLOSE TO THE MEMORY

VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT A

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*VRAM3,4 (2/4)*		
Size	Document Number	**G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 89 of 103		

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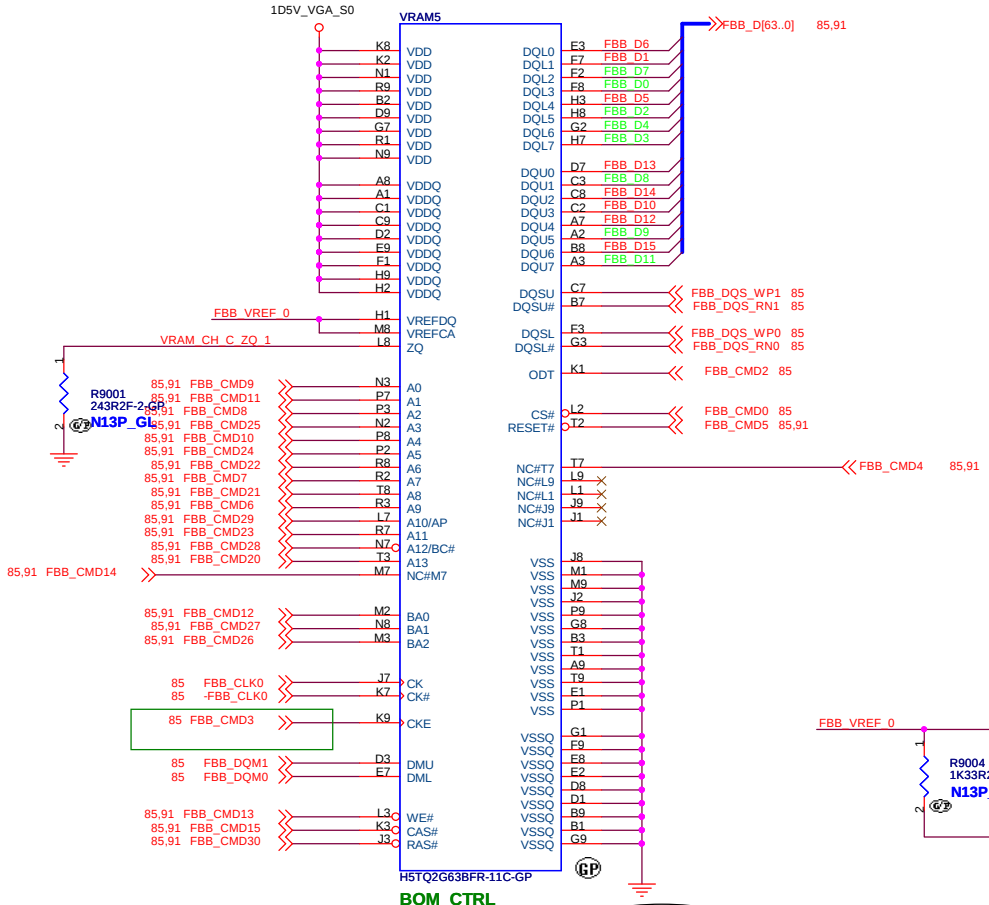
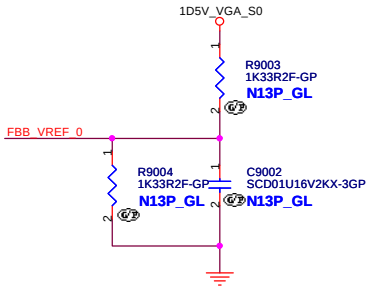
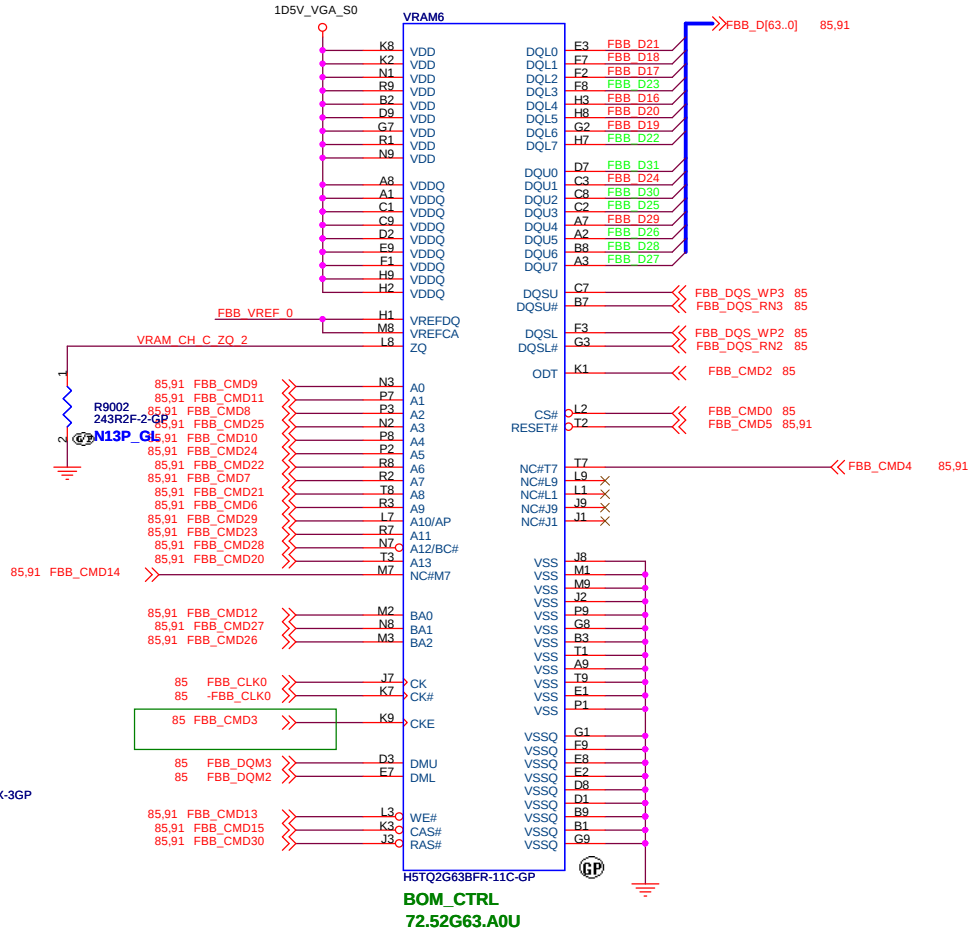
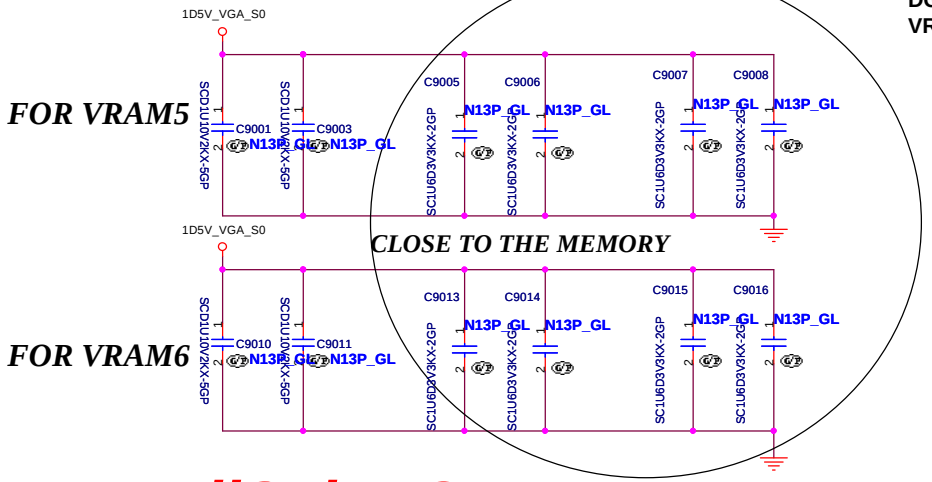
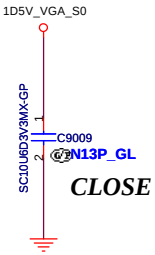






DG requires 4x0.1uF and 8x1.0uF per VRAM chip





VRAM
SAMSUNG:
K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz
K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:
H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz
H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

JV10-CS

VIDEO FRAME BUFFER PORT C

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM5,6 (3/4)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 90 of 103	

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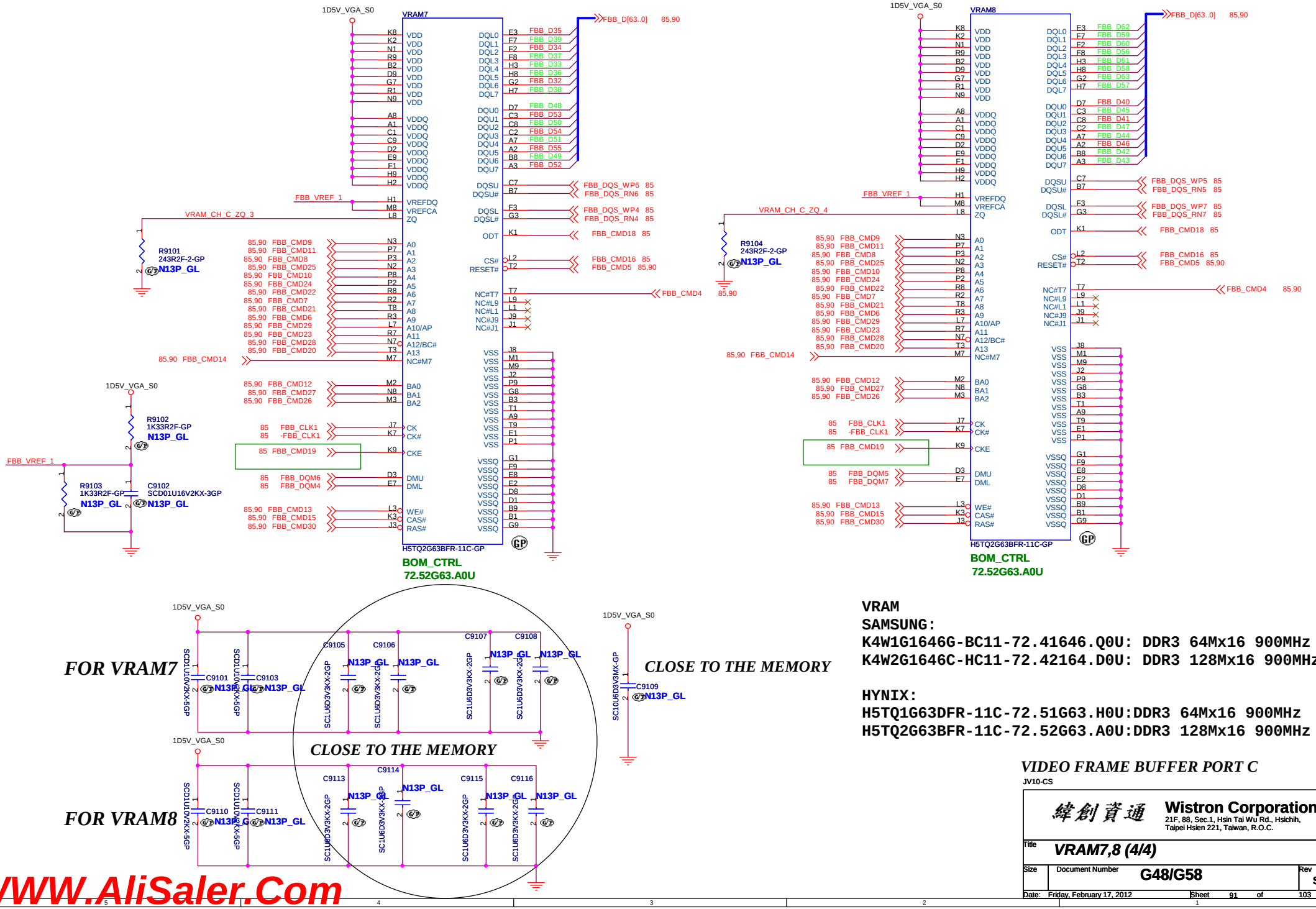

VRAM

SAMSUNG:

K4W1G1646G-BC11-72.41646.Q0U: DDR3 64Mx16 900MHz

K4W2G1646C-HC11-72.42164.D0U: DDR3 128Mx16 900MHz

HYNIX:

H5TQ1G63DFR-11C-72.51G63.H0U:DDR3 64Mx16 900MHz

H5TQ2G63BFR-11C-72.52G63.A0U:DDR3 128Mx16 900MHz

VIDEO FRAME BUFFER PORT C

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VRAM7,8 (4/4)		
Size	Document Number G48/G58		Rev SC
Date: Friday, February 17, 2012	Sheet 91 of 103		

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SSID = PWR.Plane.Regulator_VGACORE

NV_VID0-GPIO11
NV_VID1-GPIO5
NV_VID2-GPIO6
NV_VID3-GPIO1
NV_VID4-GPIO0
NV_VID5-GPIO13
NV_VID6-pull down to GND

VID[5..0]
101100 = 0.95 => N13P-GL
110010 = 0.875V => N13M-GE

Design current=

N13P-GL = 84.03660.037
N13M-GE = 84.03604.037
N13P-GL-2nd = 84.00038.A37
N13M-GE-2nd = 84.00033.037

BOM_CTRL_OPS
SIV

PU9202, PU9203 BOM CTRL

IMON
An analog output. IMON outputs a current proportional to the regulator output current.

Place near PL9201

68.R3610.20A
2nd = 68.R3610.20C

79.33719.L01
2nd = 79.33719.20L
3rd = 79.33719.2FL

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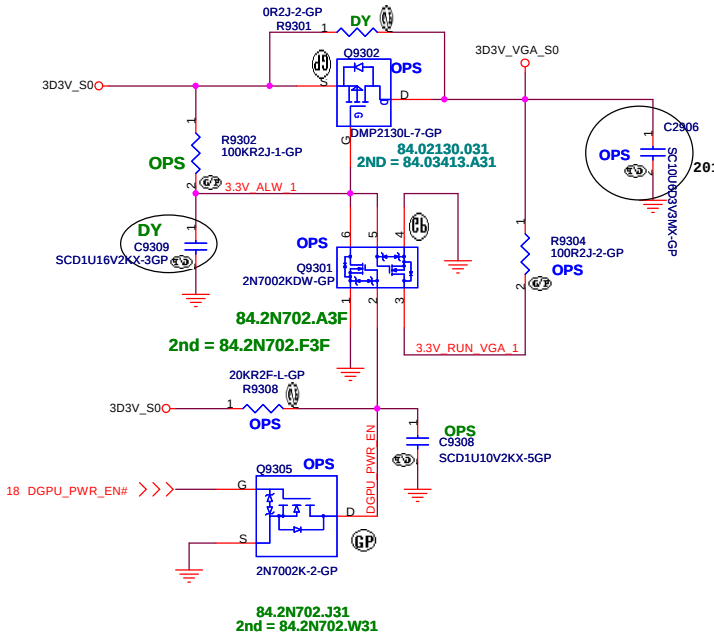
Title: ISL62882C_GPU_CORE
Size: Document Number: G48/G58 Rev: SC
Date: Friday, February 17, 2012 Sheet 92 of 103

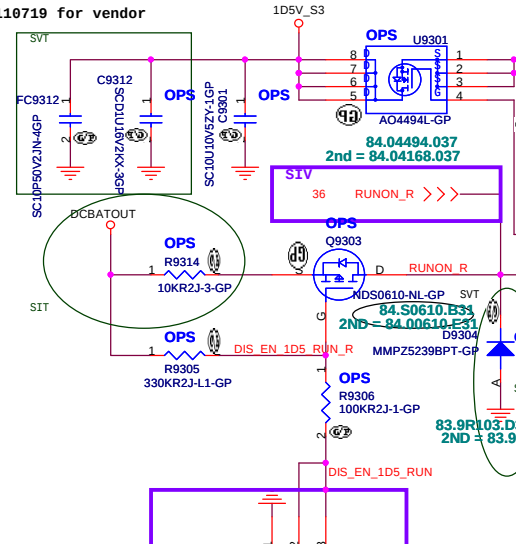
+3VS to 3.3V_DELAY Transfer



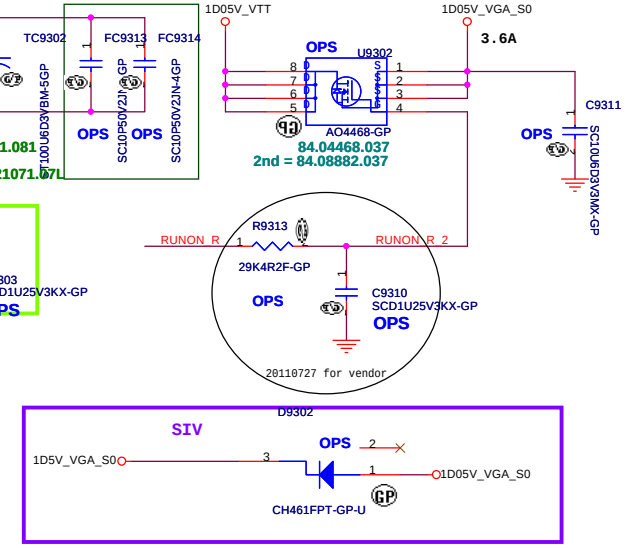
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

20110719 for vendor

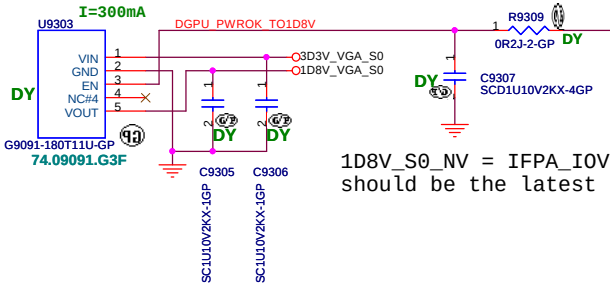
1D5V_VGA_S0



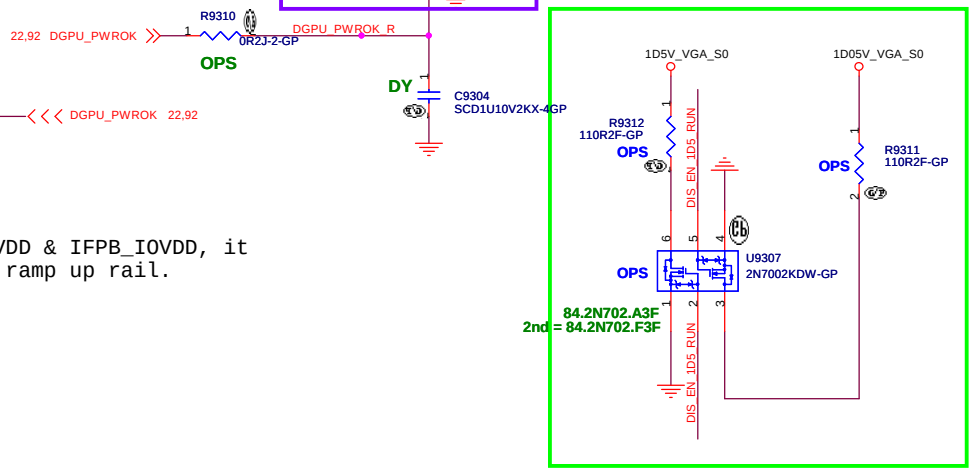
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: DISCRETE VGA POWER

Size | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 93 of 103

(Blanking)

JV10-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title	(Reserved)SW GFX LCD(1/2)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 94 of 103	

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JV10-CS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	(Reserved)SW GFX CRT(2/2)	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 95 of 103	

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Title	(Reserved)Touch panel CONN	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 96 of 103	

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CPU Plate

H3 HOLE276R178-GP — ZZ.00PAD.N11 — DY
H4 HOLE276R178-GP — ZZ.00PAD.N11 — DY
H5 HOLE276R178-GP — ZZ.00PAD.N11 — DY

VGA Std-Off

H2 STF237R128H42-GP — 34.4GD01.101 — 2nd = 34.4GD01.001 — OPS
H1 STF237R128H42-GP — 34.4GD01.101 — 2nd = 34.4GD01.001 — OPS

Check test point

3D3V_S0	AFTP1
3D3V_AUX_S5	AFTP7
3D3V_S5	AFTP8
5V_S5	AFTP9
19,27 PM_PWRBTN#	AFTP10
5,22,36 H_CPUPWRGD	AFTP11
27,36 S5_ENABLE	AFTP12
5,18,27,31,36,65,83 PLT_RST#	AFTP13

Structure boss

H6 HOLE315X315R91-S1-GP — SIT — DY — ZZ.00PAD.581
H8 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H9 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H10 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H11 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581
H13 HOLE355X355R111-S1-GP — DY — ZZ.00PAD.571
H14 HOLE315X315R91-S1-GP — DY — ZZ.00PAD.581

Spring

H16 SPRING-24-GP-U
H17 SPRING-24-GP-U
H18 SPRING-24-GP-U
H19 SPRING-52-GP
H22 SPRING-12-GP-U1
SIT

Washer

H20 SPRING-53-GP-U — G48_PLED
H21 SPRING-53-GP-U — G58_PLED

SIV

EMI Cap.

DCBATOUT
EC9719 EC9718 EC9717 EC9716 EC9715 EC9714 EC9713 EC9712 EC9711 — SCD1U50V3KX-GP
DCBATOUT
EC9705 SCD1U25V2KX-GP DY

AD+
EC9709 EC9708 — SCD1U50V3KX-GP

JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	UNUSED PARTS/EMI Capacitors	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 97 of 103	

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JV10-CS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Change-History*	
Size	Document Number **G48/G58**	Rev **SC**
Date: Friday, February 17, 2012	Sheet 98 of 103	

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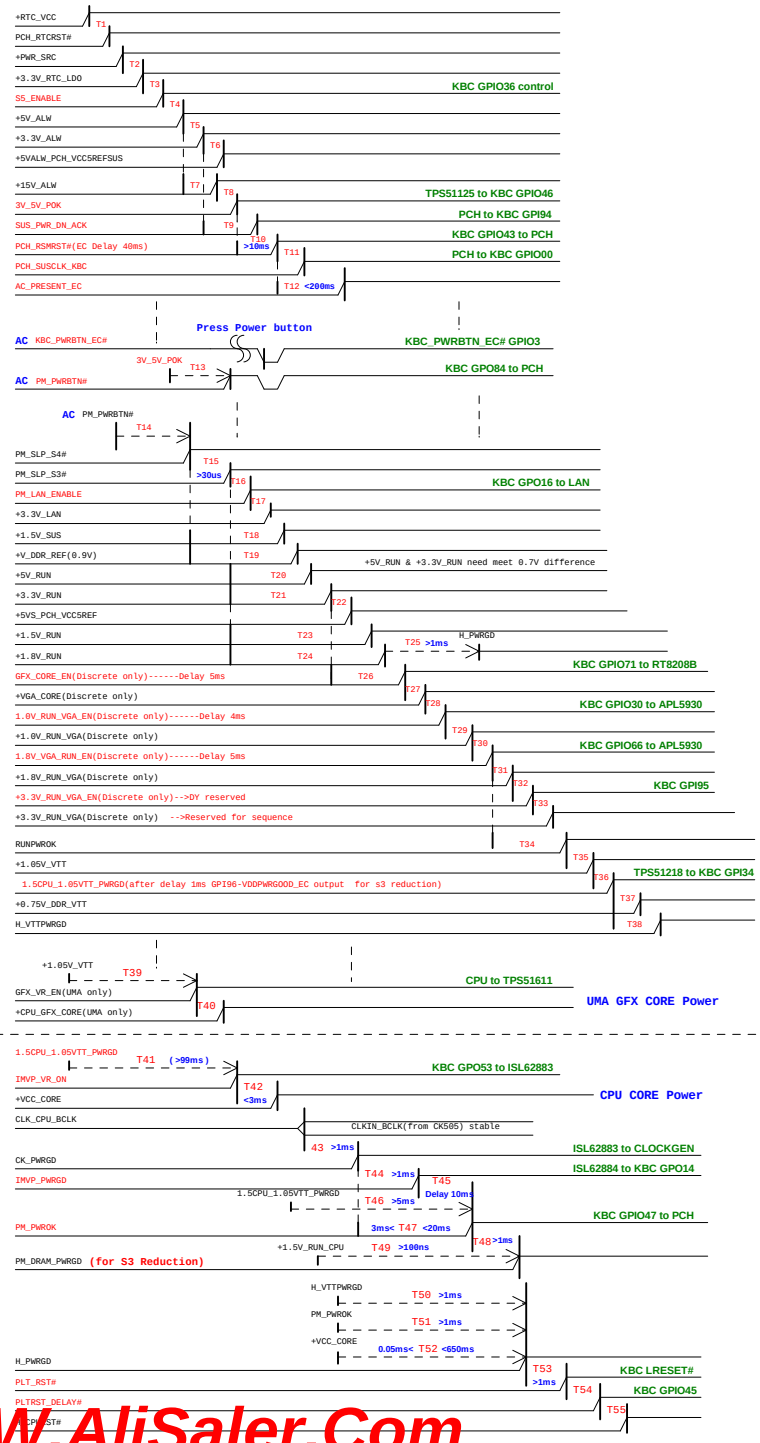
Intel-Power Up Sequence

Not Update

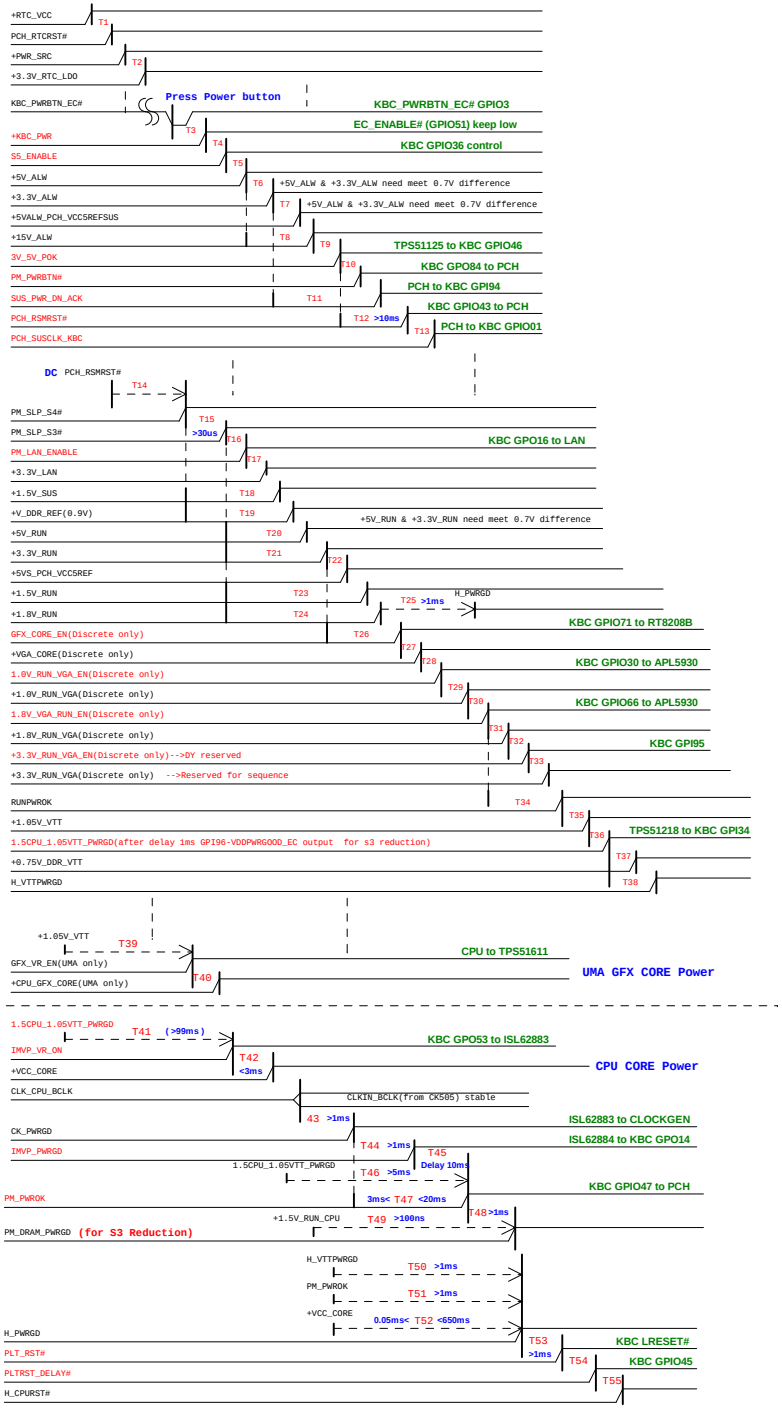
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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JVID:CS

Wistron Corporation
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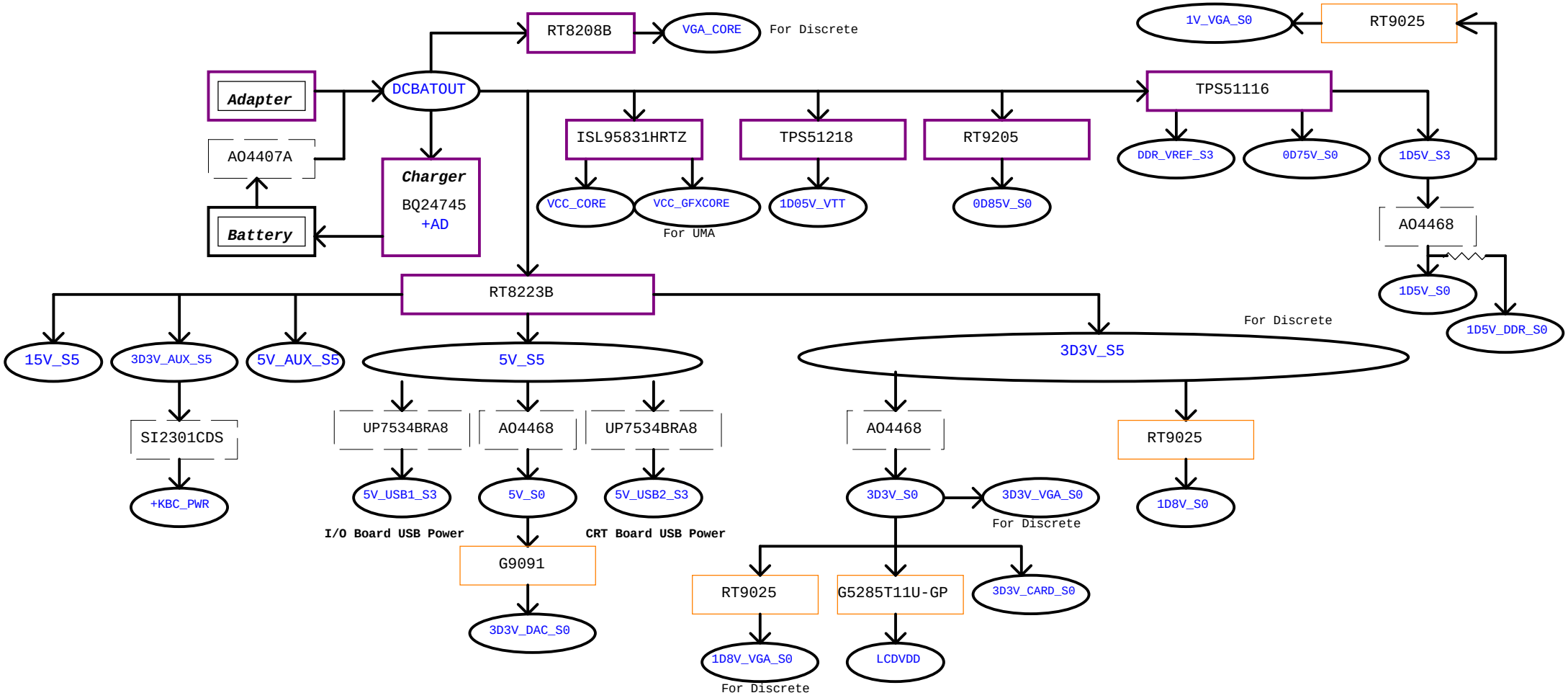
Title: Power Sequence

Size: | Document Number: G48/G58 | Rev: SC

Date: Friday, February 17, 2012 | Sheet 99 of 103

Not Update



Power Shape

Regulator	LDO	Switch

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 100 of 103

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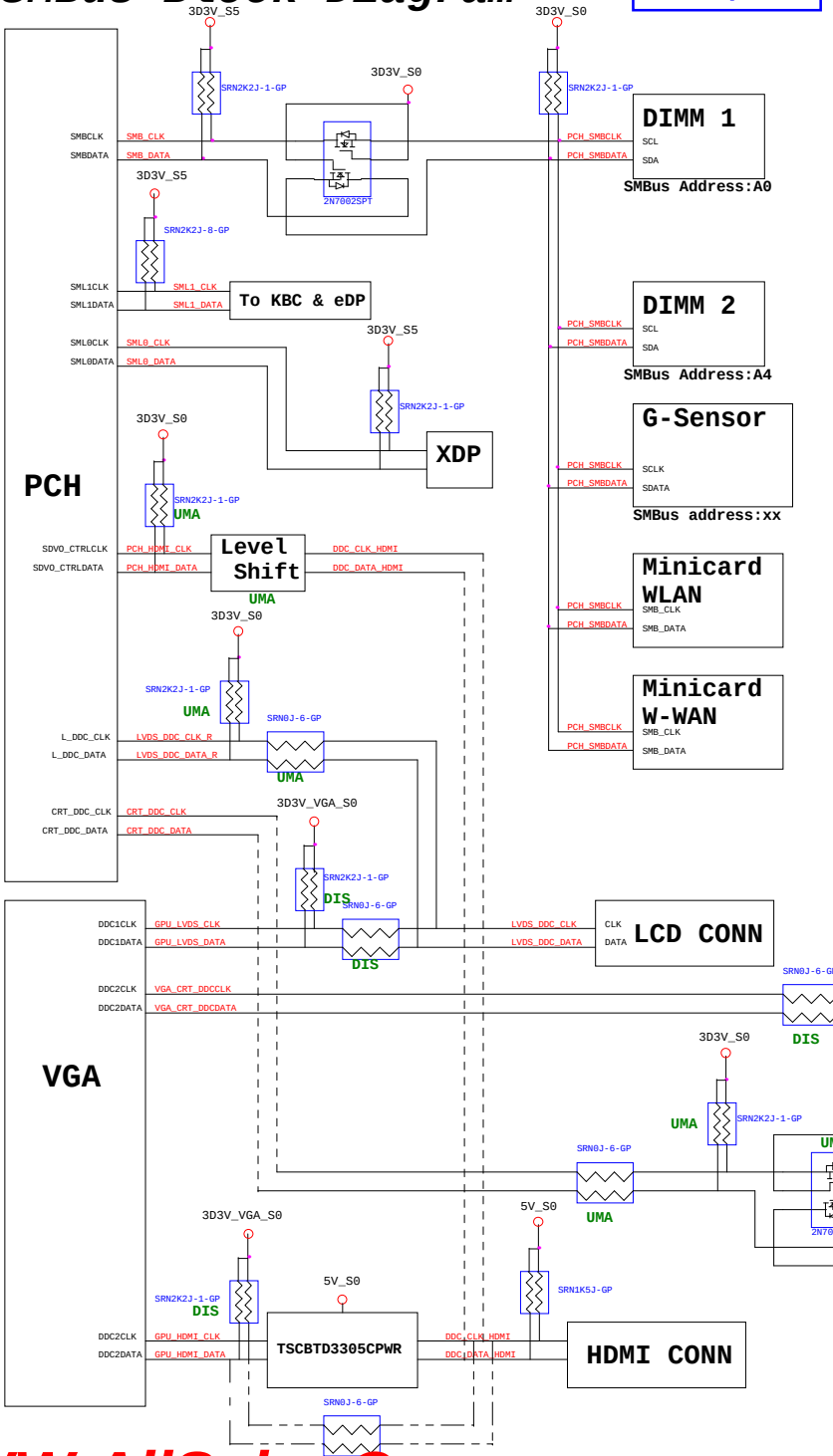
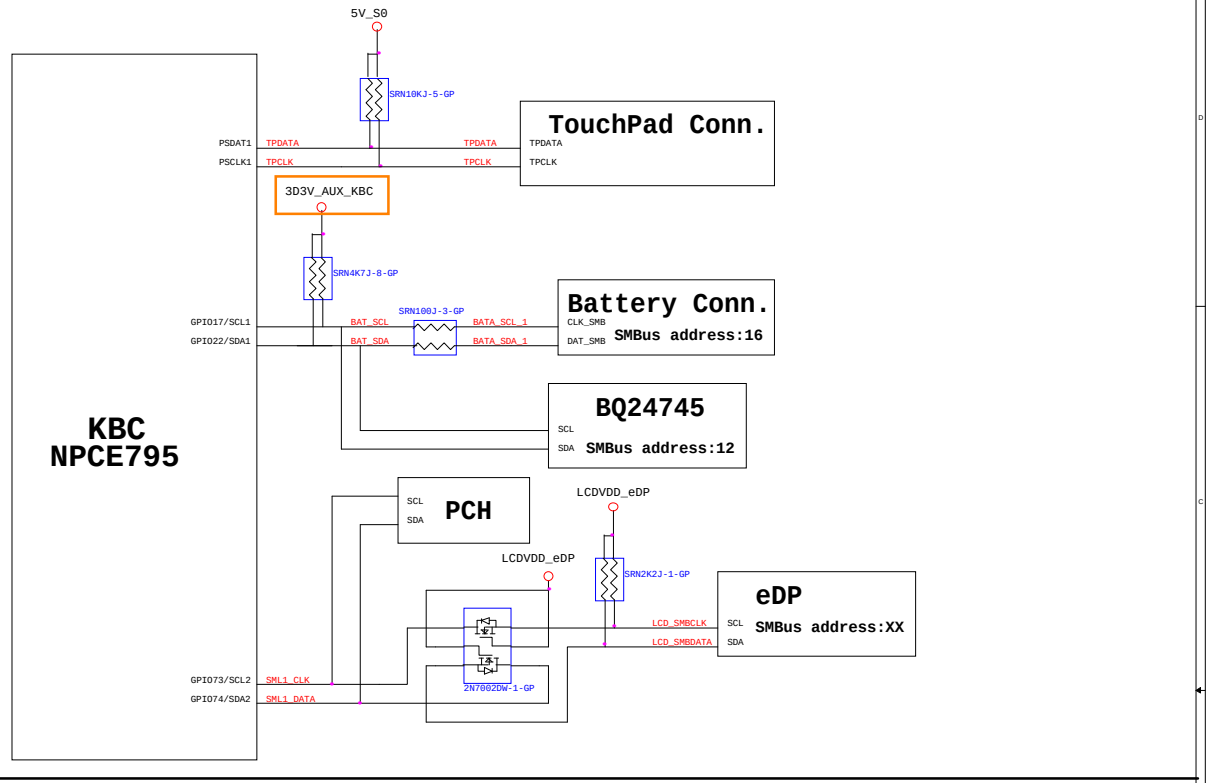
PCH SMBus Block Diagram

Not Update



KBC SMBus Block Diagram



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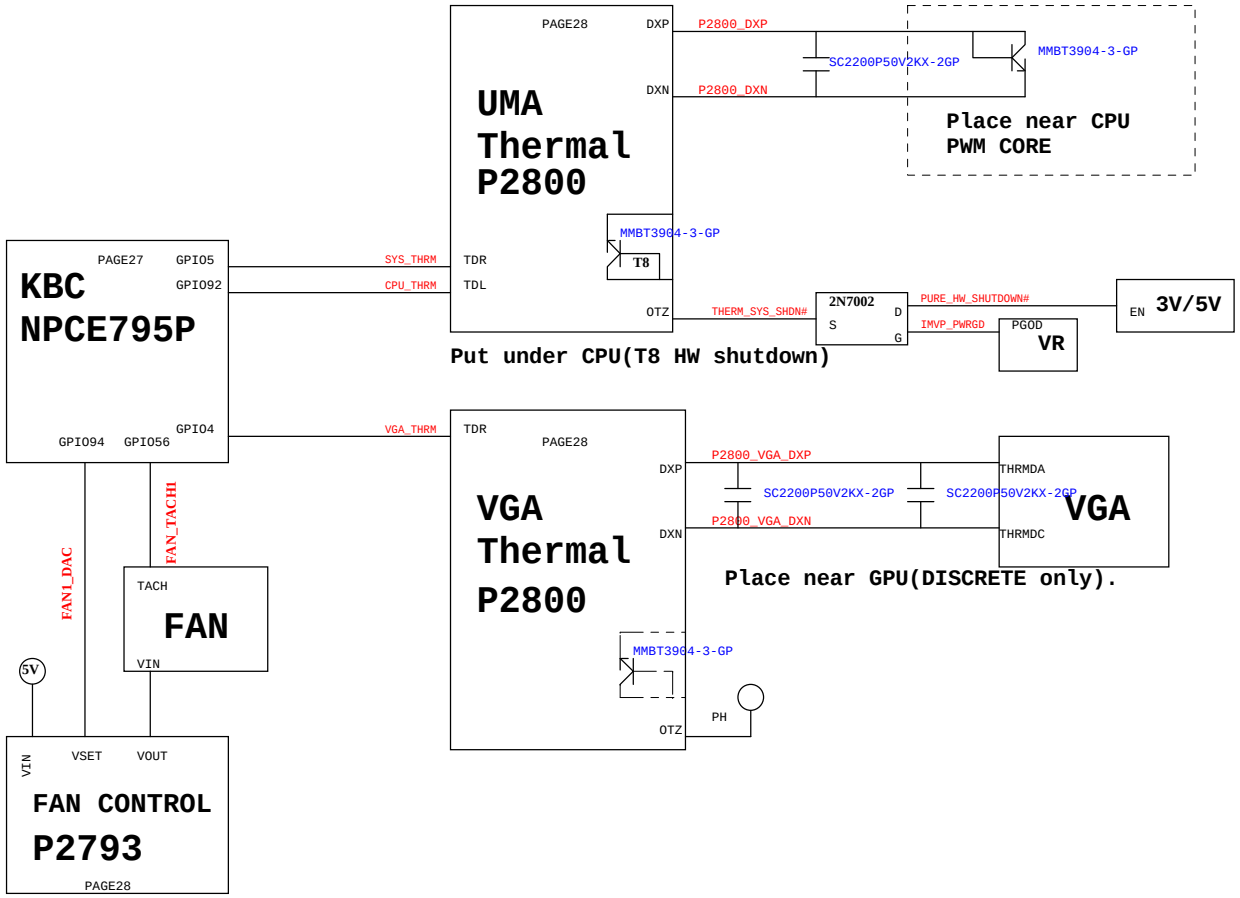
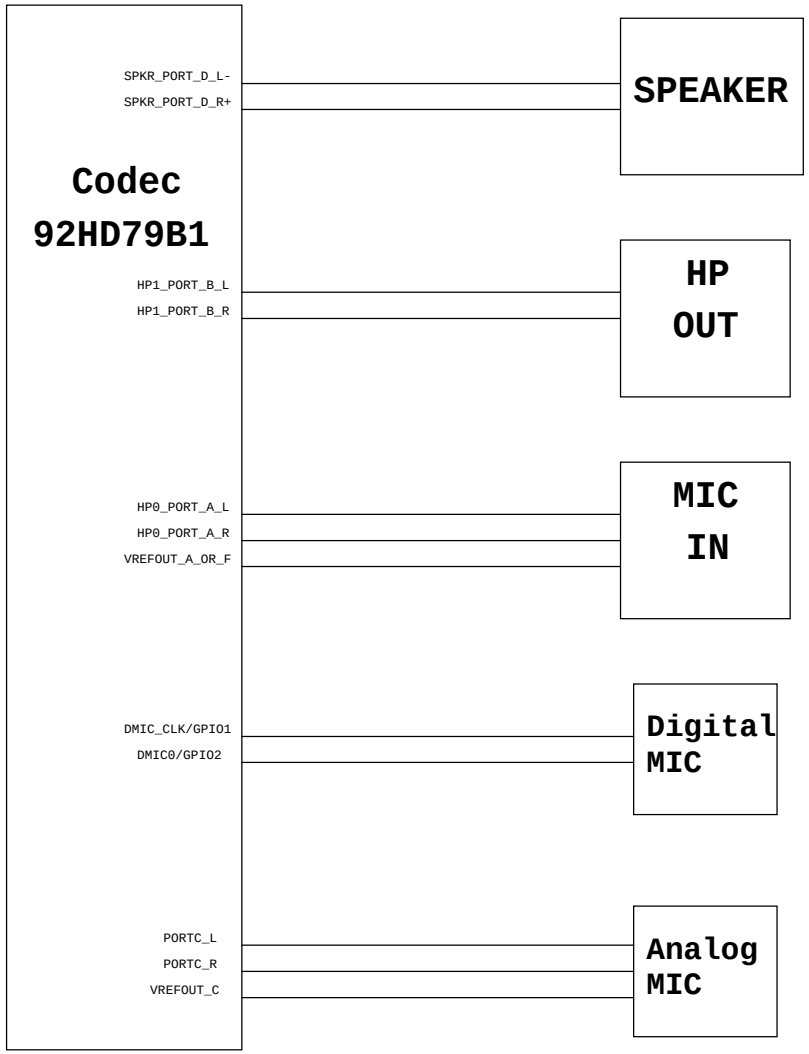
Title	SMBUS BLOCK DIAGRAM	
Size	Document Number G48/G58	Rev SC
Date: Friday, February 17, 2012	Sheet 101 of 103	

Thermal Block Diagram

Not Update



Audio Block Diagram



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Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 102 of 103

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Size	Document Number	Rev
	G48/G58	SC

Date: Friday, February 17, 2012 Sheet 103 of 103

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